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Servicehandbuch

Spektrumanalysator FSEA 20/30

1065.6000.20

Spektrumanalysator FSEB 20/30

1066.3010.20/30

ENGLISH SERVICE MANUAL FOLLOWS FIRST COLOURED DIVIDER

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6.1 Function Description

6.1.1 Instrument Function

The FSEA is a triple heterodyne receiver for the frequency range 20 Hz to 3.5 GHz. Signal processing is effected in 6 RF/IF and weighting modules, 2 synthesizer modules and a controller unit, consisting of a digital motherboard with interfaces, 468 industry PC and graphic board. The instrument can be adapted to future performance requirements by retrofitting of options in the analog and digital sections.

6.1.2 Description of the Modules (Description of the Modules in the Block Diagram

(cf. circuit diagram 1065.5000.01S)

6.1.2.1 RF Attenuator

The RF signal passes from the input socket RF Input via the input changeover switch to the switchable input attenuator, which can be switched from 0 to 70 dB in steps of 10 dB. The input signal is applied to the changeover switch as well as a 120-MHz signal which has a close-tolerance level of -40 dBm for calibration purposes or 0 dBm for the selftest of the instrument and which can be switched off.

6.1.2.2 RF Module

The RF module provides for conversion of the RF input signal to the 2nd IF (741.MHz) and for generation of the required 1st LO signal. Two microwave units are provided for the RF circuits:

- the RF converter contains the circuits for RF signal processing (filters, mixers, amplifiers)
- the YIG sampler contains generation and distribution of the 1st LO signal and the sampling mixer for synchronization of the 1st LO.

In the RF converter, the input signal passes via the input lowpass to the 1st mixer. This lowpass at the mixer input provides for suppression of the image frequency (image = LO + IF), such that the conversion remains unambiguous. In the 1st mixer the input signal is converted to an IF of 4341.4 MHz by means of the first LO (4341.4MHz bis 7841.4 MHZ). The mixer is followed by a low-noise IF amplifier, which compensates for the loss due to mixing. The signal then passes a filter with a 3-dB bandwidth of approx. 50 MHz for filtering the 1st intermediate frequency. Subsequent to the IF filter, the signal is converted to the 2nd IF of 741.4 MHz in the 2nd mixer. The local oscillator for the 2nd conversion is supplied by the 2nd IF converter module. The conversion loss of the RF module is approx. 8 dB.

6.1.2.3 2nd IF Converter

The 2nd IF converter module is used to convert the second IF to the third IF of 21.4 MHz and for generation of the second and third LO. The module has 2 inputs for IF signals which can be selected using a changeover switch. The signal from the RF converter is first amplified by approx. 15 dB, the input switch for selection of the input signal is then connected into the signal path. A power divider is provided for further processing of the IF signal with the full bandwidth of the RF converter. One output of this divider is amplified and provided as module output, the second output leads via an amplifier to a filter of 741.4 MHz with a 3-dB bandwidth of 10 MHz for further signal processing. This filter functions as resolution filter, if the resolution bandwidth is set to 10 MHz and it suppresses the image frequency which might occur with the third conversion. The filter is followed by the third mixer, which converts to 21.4 MHz. The LO for the third conversion is obtained using an oscillator which is synchronized to the 120-MHz reference of the FRAC-SYN. The signal of this VCO is also used for generation of the 2nd LO and as reference. The 2nd LO is generated by multiplication of the oscillator signal (*5) and filtering of the comb line. The conversion gain of the converter is typical 12 dB, the level in relation to the input mixer is approx. +4 dB.

6.1.2.4 IF Filter

The resolution filters for bandwidths between 1 kHz and 5 MHz are located on the IF filter board. With 10 MHz bandwidth the filter stages of the module are bypassed. Crystal filters are used for bandwidths from 1 kHz to 30 kHz, LC filters are used for bandwidths of 50 kHz or above. The individual models of the FSE family are supplied with two different models of the IF filter board. The models 20 (e.g., FSEA 20) provide four filter stages, the models 30 provide five ones. The individual filter stages have been decoupled from each other by means of amplifiers which is why they act like a Gaussian filter. In comparison to other types of filter, the Gaussian filter provides minimum settling time.
The two models of IF filter accommodate switchable IF amplifiers (step gain), and two independent calibration amplifiers subsequent to the first two filter stages. The step gain can be switched in 0.1-dB steps from 0 to 50 dB and is used to increase the signal on the reference level in spite of different levels at the input mixer.
Amplification of step gain = -10dBm - (mixer level)
One of the two calibration amplifiers is used to compensate for the deviations of amplification with different bandwidth or step gain settings. This amplifier is controlled via the serial interface of the level transputer and a D/A converter on the IF filter board. The second calibration amplifier is controlled by an analog voltage, which is modified by the frequency transputer during the sweep according to the frequency response of the input stages.
The module provides two outputs which the filtered, third IF is applied to. The output level in relation to a signal on the reference level is 0 dB, as long as step gain can be adjusted (mixer level >= -60dBm). One output is connected to the rear panel, the second one to the digital IF board, where bandwidths between 10 Hz and 1 kHz have been realized.
In parallel, the logarithmic value of the IF signal on the board is determined. The log module consists of an integrated, series-connected rectifier which provides for a dynamic of 90 dB in the models 20 and 110 dB in the models 30. The generated video signal is applied to a 20-MHz A/D converter on the detector board where it is looped through to the rear panel.

6.1.2.5 Detector Board

The detector board contains the A/D converter for acquisition of analog measured values. The converter is followed by a correction memory, where the characteristic of the log module is linearized. Optionally, a delogarithmation can be performed in this correction memory which allows for linear representation of the measured values. A gate array is provided for video filtering of the corrected measured values, subsequently, the digital selection of the detectors is made (detector-LCA: samples, peak, average, RMS). Besides, the board provides for triggering of the sweep to internal and external trigger events (trigger LCA). With fast acquisition of measured values (20 MHz), the values are stored in the test RAM (128k*16bit) for subsequent off-line evaluation in the transputer (FAST RAM). The selftest A/D converter provides for processing of the diagnosis/selftest results for the various analog boards. The serial instrument-bus master controls the analog boards in the signal path.

6.1.2.6 Digital IF

The signal path via the log module is not used with resolution bandwidths < 1kHz. The signal is still filtered to a bandwidth of 3 kHz by the IF filter board, however, it is then converted to an IF of 25 kHz and filtered digitally. An 18-bit A/D converter is provided on the digital IF board for sampling with 25 kHz. The level must be reduced by approx. 20 dB across the entire signal path in order to obtain the same intermodulation-free dynamic range as is obtained with the analog log module. The digital IF contains an amplifier which is switchable from 0 to 20 dB in order to provide the optimum dynamic range for the D/A converter.

6.1.2.7 FRAC-SYN

The FRACSYN module contains reference-frequency conditioning of the instrument, the interpolation synthesizer for YIG synchronization and a calibration source.
The FRACSYN module has the following functions:
- Generation of reference frequencies 10, 20, 30, 60 and 120 MHz
- Generation of a calibration signal
- Synchronization of the YIG oscillators by means of the interpolation synthesizer
- Control of further boards via a serial interface

Three high-frequency local oscillators are required in the FSE, a simplified block diagram illustrates their theory of operation. The first LO, which can be tuned in the range from 4341.4 MHz to 7841.4 MHz as well as the fixed-frequency LOs with 720 MHz and 3600 MHz are synchronized to a crystal oscillator at 120 MHz, which is again synchronized to a frequency-stable reference oscillator (TCXO with 10 MHz in the basic instrument, OCXO with Low Phasenoise option). If the instrument is switched to external reference, the 120-MHz oscillator is synchronized to this signal via a programmable divider. The divider can be adjusted such that reference frequencies from 1 to 16 MHz can be synchronized to in steps of 1 MHz.
The first LO is based on a YIG oscillator, which can be tuned in the frequency range of interest. Coarse tuning of the YIG oscillator is made via a D/A converter and a voltage-controlled current source. The FRACSYN board supplies a signal between 475 MHz and 700 MHz which can be set with any stepsize whatsoever (< 0.1 mHz).
The sample signal is amplified in the YIG sampler on the RF module and down-converted with the output frequency of the YIG oscillator via a sampling mixer. The offset between the calculated comb line and the pretuning is set to 30 MHz. The output signal of the sampler is locked to 30 MHz via the control section of the YIG. The YIG is thus synchronized to the corresponding comb line of the FRACSYN signal. The phase comparison is made on the FRACSYN which also contains the loop filter, using a discriminator.

6.2 Service and Selftest Functions

The following measures have been taken to allow for error localization by means of the selftest functions:

Each synthesizer and signal module contains one or two 1-out-of-8 analog multiplexer(s), which select(s) up to 16 test voltages via buffer amplifier. The test voltages are output to the common selftest channel. Various functions can be checked:

- supply voltages generated on-board
- operating points of amplifiers
- signal levels by means of level detectors

Selection of the test channel is made via the serial board control. All instrument settings required for checking a test function are made automatically.

A differentiation has to be made between:

- permanent selftest functions
- the user selftest
- the service test

6.2.1 Permanent Selftest

The permanent selftest consists of supervising the synthesizer loops and the operating voltages in the power supply unit.

a) Supervision of the synthesizer and reference frequencies:

It is checked with all loops during operation, whether the tuning voltages are within the permitted tolerance. The LO amplifier outputs are checked with regard to adherence to the required output levels, occurrence of overload is recognized by means of level detectors located in the signal path at suitable places. All supervisory circuits work as OPEN collector outputs to common interrupt lines, the error-indicating board is localized by the controller by reading the status registers on the boards. Several interrupt lines have been provided for these supervisory tasks:
LO-Unlock for supervision of the frequency PLLs
LO-Level for supervision of the LO levels
IF-OVR for supervision of the 2nd IF overload
RF-OVR for supervision of the RF and 1st IF overload
If a faulty function has been found, the user is informed by a system message. One or more of the following error messages is then displayed:

Message	**Meaning**
- Reference unlock	Reference oscillator not synchronized
- 1st LO unlock	First LO not synchronized
- 2nd/3rd LO unlock	Second and third LO not synchronized
- Level 1st LO	LO level at first mixer too small
- Level 2nd LO	LO level at second mixer too small
- Level 3rd LO	LO level at third mixer too small
- RF OVR	Input signal too large
- IF OVR	Signal following IF amplifier too large

b) Supervision of the power supply function:

All supply voltages are checked with regard to adherence to their tolerances. Correct functioning is indicated at the rear panel of the instrument by the SUPPLY CHECK LED. A shortcircuit on any of the supply voltages causes switch-off of the power supply.

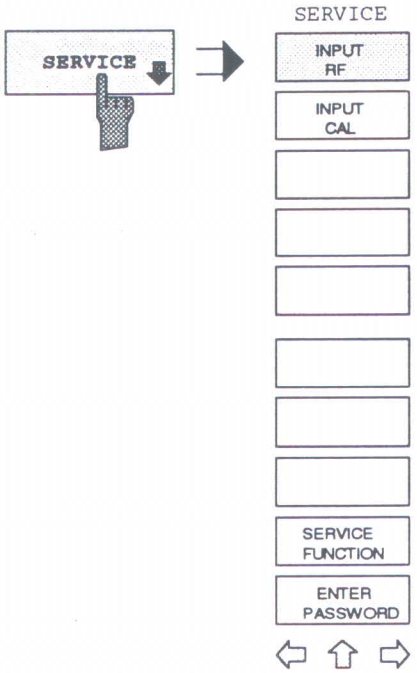
6.2.2 User Selftest

The user selftest checks the adherence to the rated values at the selftest points on all boards. First, all LO signals and, then, the signal path of the instrument is checked. Operating instructions for the selftest can be looked up in the Operating Manual, Section 2.4.4.3.

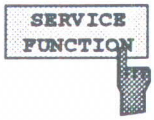
6.2.3 Service Selftest

The service selftest allows for specific check of circuitry on individual boards. This test is only accessible after entry of the password.

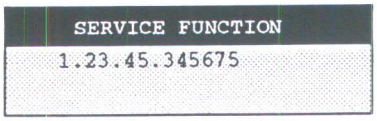
Upon entry of the password. a menu is displayed with calling the selftest, which is more extensive than the user selftest menu:



The FSE contains a number of service functions which would impair the analyzer functions if applied inappropriately. These functions are normally disabled and are not enabled until entering the *PASSWORD*.



The *SERVICE FUNCTION* softkey calls various service functions. The individual functions are described in the subsequent section.



The selection of the service function is made according to the following nomenclature:

Service function: gg.bb.ff.p1.p2

gg Number of function group:
0: general
1: means boards/functions which are controlled by the 486 processor
2: means boards/functions which are controlled by the transputers (particularly analog modules)

bb Board number, presently reserved:

0	Functions which are performed simultaneously on all boards
1	Grafic Board
2	CPU Board
3	Dig. Motherboard
4..9	reserved
10	FRAC SYN
11	RF Module
12	2nd IF Converter
13	LO Phase
14	Preselector
15	Tracking Gen
16	MW Converter
17	MW YIG Filter
18	reserved
19	FSET-Z1-FT
20	Detector
21	RF Attenuator
22	TG Attenuator
23	Dig. IF Board
24	I/Q Demod
25	Channel Filter
26	IF-Filter
27	FSET-Z1-PT
28	FSET-IF1
29	FSET-IF2
30	FSET-IF741
31	FSET-Video
32...	reserved

ff — Function number:
number of service function assigned to the module. The number "0" has been reserved for switching off all active service functions on the module selected under bb (if required and if possible). The numbers "1 to 19" select functions which have been realized equally for all modules (e.g., read-out of the analog multiplexers), however, which differ in the following parameters and/or are to be performed on the selected module, only.

p1 — Parameter 1 (optional)
1st parameter for entered service function, entry range:.
-2147483648 to +2147483647 (32-bit integer, signed)

p2 — Parameter 2 (optional)
2nd parameter for entered service function, entry range:
-2147483648 .... +2147483647 (32-bit integer, signed)

Note: *Shortly switch off the analyzer and on again to make sure that the activated service function is switched off. Inidvidual functions can be switched off using the reserved function code 0.*
PRESET normally does not reset any service function.
Parameters which have not been entered are assigned 0.
Examples:
2.10
FRACSYN module, function=0, parameter1=0, parameter2=0
2.10..4
FRACSYN module, function=0, parameter1=4, Parameter2=0

Note: *The softkey is not provided until entering the SECURITY CODE.*

6.2.3.1 List of Service Functions

Function Group 0 (General Functions)

Function	Parameter	Function description

Function Group 1 (486 Section)

Function	Parameter	Function description
Software 0.0.xx		
1.0.0 Identification of model and availability of options	Parameter 1: 0 Transputer request 1 Setting of FSEA 2 Setting of FSEB 3 Setting of FSEM 4 Setting of FSEL 5 Setting of FSEIA 6 Setting of FSEIB 7 Setting of FSEIM 8 Setting of FSET Parameter 2 (optional): 10 Model 10 20 Model 20 30 Model 30 If parameter 2 unequals 10, 20 or 30, model 30 is used	Requesting or setting of the module options
Grafic Board 1.1.xx		
CPU Board 1.2.xx		
Dig. Motherboard 1.3.xx		

Function Group 2 (Transputer/Analog Modules)

The subsequent table contains all service functions which simultaneously affect all modules:

Function	Parameter	Function description
all boards 2.0.xx		**Functions for all boards**
2.0.1	-	This function causes an interrupt reset to be released on all boards (singular LOW pulse)
2.0.2	Parameter 1: 0 Restore Flags 1 CalCorr 2 CalBWData 3 CorrRAMData 4 CalLevelData 5 CalTempData 6 CalLOSupData 7 CalIQData 8 FreqCorrRF 9 FreqCorrSC 10 FreqCorrPreSel 11 FreqCorrPreAmp 12 FreqCorrRFAtt 13 FreqCorrMWConv 14 FreqCorrMWYig 15 FreqCorrMWDiplx 20 CalHighSpeed Parameter 2: 0 = OFF 1 = ON	This function allows for switching on or off (part of) the calibration data. Parameter 1 indicates which calibration data is to be switched, parameter 2 specifies the switching direction (ON, OFF). The setting thus selected can be overwritten by the system at any time. If parameter 1 is assigned the value 0, the complete flag structure is reset to the setting which prevailed prior to the first manipulation by this function.

The subsequent table contains all service function numbers which have been realized equally for all boards, however, which refer to one single board, only. These functions may be missing with individual boards due to the hardware configuration, which is why they are listed in the board-specific tables again, if they are provided with the respective board:

Function	Function description
2.bb.0	Switching off of all service functions started for the respective board. This includes stopping of of running cyclic functions as well as enabling of disabled/modified system parameters.
2.bb.1	This function cyclically reads out a channel of the respective onboard diagnosis multiplexer selected via the parameter 1 and displays the result. Up to eight different channels on different boards can be read out and displayed, simultaneously. The repeated entry of a channel number terminates the measurement and output for just this channel. Entering the function 2.bb.0 terminates all active channel outputs for the selected board.
2.bb.2	This function cyclically reads out the status register of the selected board and displays the contents in binary form. The status register of one single board can be read out at a time, only. If the status register of another board is requested to be output, the read-out for the previously selected status register is stopped before. The function 2.bb.0 terminates the readout of the status register.
2.bb.3	This function enables reading the EEPROMs of a board into a file of the file system (CAL group) or loading new data from a file of the file system into the EEPROMs. Parameter 1 = 0: reading out the EEPROMs Parameter 1 = 1: programming the EEPROMs
2.bb.4	This function allows for modifying various parameters of the EEPROM header block of a board. The modificatons are stored in the EEPROM immediately! Parameter 1 is used to select the header parameter which is to be varied, parameter 2 contains the new value for the parameter to be varied.
2.bb.5	This function programs all data from the EEPROM buffer in the RAM into the EEPROM of the respective board.
2.bb.6	This function reads out the latest bit pattern which has been programmed into the control register of a board from the RAM copy of the hardware setting and displays it in binary (incl. subaddress) as well as in decimal form. Parameter 1indicates the bus address of the register to be output, parameter 2 determines the subaddress (offset starting at 0, not the weighted bit pattern), if required. The service functions 2.bb.7 and 2.bb.8 subsequently refer to these information!
2.bb.7	This function writes the bitpattern transferred in parameter 2 into the register selected by function 2.bb.6 at the bit positions given via the mask in parameter 1. The bits thus marked are subsequently disabled for system access. They can be enabled again for *all* registers onboard using the function 2.bb.0 or for the register selected under 2.bb.6, only, using the function 2.bb.8. Active bits in the mask have to be set to 1. Using this function again for the same register, however, using another mask, partly releases a disabled access!
2.bb.8	This function reenables the register selected by 2.bb.6 for system access.

The subsequent tables contain all service functions which are presently provided for the various boards:

Function	Parameter	Function description
FRAC SYN 2.10.xx		**FRAC SYN module**
2.10.0		Deletion of all active service functions on this board
2.10.1	Number of the multiplexer channel to be read out	cyclical readout of the analog-multiplexer channel. Repeated entry of the same channel terminates the readout for this channel.
2.10.2	-	cyclical output of the status register of the board
2.10.3	p1 = 0: readout of the EERPOMs p1 = 1: programming of the EEPROMs	This function enables reading the EEPROMs of the FracSyn into the FRAC_SYN.DAT file of the file system (CAL group) or loading new data from this file into the EEPROMs.
2.10.4	p1: value[0..2] p2: value[0..99]	This function allows for modifying various parameters of the EEPROM header block of the board. p1 = 0: type of board, p1 = 1: main modification index p1 = 2: temporary modification index p2 new value for the entry
2.10.5	-	This function programs all data from the EEPROM buffer in the RAM into the EEPROM of the respective board.
2.10.6	p1: bus address p2: sub address	This function reads out the latest bit pattern which has been programmed into the control register of a board from the hardware and displays it.
2.10.7	p1: bitpattern mask p2: bit pattern new value	This function writes the bitpattern transferred in parameter 2 into the register selected by function 2.10.6 at the bit positions given via the mask in parameter 1. The bits thus marked are subsequently disabled for system access.
2.10.8	-	This function reenables the register selected by 2.10.6 for system access.
2.10.20	p1: value [0...4095] p2=0: modification only p2=1: modification and reading to the EEPROM	This functiobn allows for modifying the D/A converter for adjustment of the reference frequency.
2.10.21	p1 = 0: CalGen off p1 = 1: CalGen on p2 = Cal level in dBm	This function switches over the calibration source. The setting made is locked for system access. Release via 2.10.0.

Function	Parameter	Function description
RF module 2.11.xx		**RF Module**
2.11.0		Deletion of all active service functions on this board
2.11.1	Number of the multiplexer channel to be read out	cyclical readout of the analog-multiplexer channel. Repeated entry of the same channel terminates the readout for this channel.
2.11.3	p1 = 0: readout of the EEPROMS p1 = 1: programming of the EEPROMs	This function enables reading the EEPROMs of the RF module into the RF.DAT file of the file system (CAL group) or loading new data from this file into the EEPROMs.
2.11.4	p1: value[0..2] p2: value[0..99]	This function allows for modifying various parameters of the EEPROM header block of the board. p1 = 0: type of board, p1 = 1: main modification index p1 = 2: temporary modification index p2 new value for the entry
2.11.5	-	This function programs all data from the EEPROM buffer in the RAM into the EEPROM of the respective board.
2.11.6	p1: bus address p2: subaddress	This function reads out the latest bit pattern which has been programmed into the control register of a board from the RAM copy of the hardware setting and displays it.
2.11.7	p1: bit pattern of mask p2: bit pattern of new value	This function writes the bitpattern transferred in parameter 2 into the register selected by function 2.11.6 at the bit positions given via the mask in parameter 1. The bits thus marked are subsequently disabled for system access
2.11.8	-	This function reenables system access to the register selected by 2.11.6.
2.11.20	p1 = 0: NoiseGen off p1 = 1: NoiseGen on	This function switches over the noise generator. The setting made is then locked for system access. Release via 2.11.0.
2.11.21		This function accepts the DAC setting values for the LO suppression and reads them to the EEPROM onboard.
2.11.22	p1 = -1: reading out the total attenuation error p1 = [0..700/1400]: reading out a level-correction value from the level-correction list of the FSEA/FSEB.	Readout of an EEPROM parameter from the RAM copy of the hardware setting and output on the display: p1: address or ID of the EEPROM parameter to be read out
2.11.23	p1 = -1: writing the total attenuation error to the RAM p1 = [0..700/1400]: writing a level correction value into the level-correction list of the FSEA/FSEB. p2: [0..255]	Overwriting an EEPROM parameter in the RAM copy of the hardware setting, updating the interpolation lists for the level correction and status output on the display: p1: address or ID of the EEPROM parameter to be overwritten p2: new value for the selected EEPROM parameter

Function	Parameter	Function description
2nd IF Converter 2.12.xx		**2nd IF Converter**
2.12.0		Deletion of all active service functions on this board
2.12.1	Number of the multiplexer channel to be read out	cyclical readout of the analog-multiplexer channel. Repeated entry of the same channel terminates the readout for this channel.
2.12.2	-	cyclical output of the status register of the board
2.12.3	p1 = 0: readout of the EEPROMS p1 = 1: programming of the EEPROMs	This function enables reading the EEPROMs of the2nd_IF_Converter into the SCND_IF.DAT file of the file system (CAL group) or loading new data from this file into the EEPROMs.
2.12.4	p1: value[0..2] p2: value[0..99]	This function allows for modifying various parameters of the EEPROM header block of the board. p1 = 0: type of board, p1 = 1: main modification index p1 = 2: temporary modification index p2 new value for the entry
2.12.5	-	This function programs all data from the EEPROM buffer in the RAM into the EEPROM of the respective board.
2.12.6	p1: bus address p2: subaddress	This function reads out the latest bit pattern which has been programmed into the control register of this board from the RAM copy of the hardware setting and displays it.
2.12.7	p1: bit pattern of mask p2: bit pattern of new value	This function writes the bitpattern transferred in parameter 2 into the register selected by function 2.12.6 at the bit positions given via the mask in parameter 1. The bits thus marked are subsequently disabled for system access.
2.12.8	-	This function reenables system access to the register selected by 2.12.6.
2.12.20.p1.p2	p1: value [0...255] p2=0: modification only p2=1: modification and reading to the EEPROM	This function allows for modifying the D/A converter DAC0 for adjustment of the OVR1 threshold
2.12.21.p1.p2	p1: value [0...255] p2=0: modification only p2=1: modification and reading to the EEPROM	This function allows for modifying the D/A converter DAC1 for adjustment of the OVR1-10 threshold
2.12.22.p1.p2	p1: value [0...255] p2=0: modification only p2=1: modification and reading to the EEPROM	This function allows for modifying the D/A converter DAC2 for adjustment of the OVR2 threshold
2.12.23.p1.p2	p1: value [0...255] p2=0: modification only p2=1: modification and reading to the EEPROM	This function allows for modifying the D/A converter DAC3 for adjustment of the OVR2-10 threshold
2.12.27.p1.p2	p1: value [0...255] p2=0: modification only p2=1: modification and reading to the EEPROM	This function allows for modifying the D/A converter DAC7 for adjustment of the VCO frequency
2.12.28		This function initiates the VCO calibration of the third LO. With normal operation of the instrument, this calibration is performed with total calibration, only.

Function	Parameter	Function description
LO Phase 2.13.xx		**LO Phase module**
2.13.0		Deletion of all active service functions on this board
2.13.1	Number of the multiplexer channel to be read out	cyclical readout of the analog-multiplexer channel. Repeating the entry of the same channel terminates the readout for this channel.
2.13.2		-
2.13.3	p1 = 0: readout of the EEPROMS p1 = 1: programming of the EEPROMs	This function enables reading the EEPROMs of the LO_Phase module into the LO_PHASE.DAT file of the file system (CAL Group) or loading new data from this file into the EEPROMs.
2.13.4	p1: value[0..2] p2: value[0..99]	This function allows for modifying various parameters of the EEPROM header block of the board. p1 = 0: type of board, p1 = 1: main modification index p1 = 2: temporary modification index p2 new value for the entry
2.13.5	-	This function programs all data from the EEPROM buffer in the RAM into the EEPROM of the respective board.
2.13.6	p1: bus address p2: subaddress	This function reads out the latest bit pattern which has been programmed into the control register of this board from the RAM copy of the hardware setting and displays it.
2.13.7	p1: bit pattern of mask p2: bit pattern of new value	This function writes the bitpattern transferred in parameter 2 into the register selected by function 2.13.6 at the bit positions given via the mask in parameter 1. The bits thus marked are subsequently disabled for system access.
2.13.8	-	This function reenables system access to the register selected by 2.13.6.

Function	Parameter	Function description
MW Converter 2.16.xx		**MW Converter**
2.16.0		Deletion of all active service functions on this board
2.16.1		-
2.16.2		-
2.16.3	p1 = 0: readout of the EEPROMS p1 = 1: programming of the EEPROMs	This function enables reading the EEPROMs of the MW Converter into the MW_CONV.DAT file of the file system (CAL Group) or loading new data from this file into the EEPROMs.
2.16.4	p1: value[0..2] p2: value[0..99]	This function allows for modifying various parameters of the EEPROM header block of the board. p1 = 0: type of board, p1 = 1: main modification index p1 = 2: temporary modification index p2 new value for the entry
2.16.5	-	This function programs all data from the EEPROM buffer in the RAM into the EEPROM of the respective board.
2.16.6	p1: bus address p2: subaddress	This function reads out the latest bit pattern which has been programmed into the control register of this board from the RAM copy of the hardware setting and displays it.
2.16.7	p1: bit pattern of mask p2: bit pattern of new value	This function writes the bitpattern transferred in parameter 2 into the register selected by function 2.16.6 at the bit positions given via the mask in parameter 1. The bits thus marked are subsequently disabled for system access.
2.16.8	-	This function reenables system access to the register selected by 2.16.6.
2.16.20		This function sets the synthesizer to zero span and sets frequency conditioning to FB > 7GHz. No limitation of the maximum frequencies.
2.16.21	p1: value [0...255] p2=0: modification only p2=1: modification and storing in the RAM copy of the hardware setting	Parameter 1:frequency correction of YIG-Filter
2.16.22	p1: value [0...16383] p2=0: modification only p2=1: modification and reading to the EEPROM	Parameter 1: DAC value for start-frequency correction
2.16.23	p1: value [0...16383] p2=0: modification only p2=1: modification and reading to the EEPROM	Parameter 1: DAC value for stop-frequency correction
2.16.24	-	Extracts the required EEPROM data from the current hardware buffer and programs them into the EEPROM (for 2.16.21/22/23)
2.16.25	p1 = 0: 7..15GHz p1 = 1: 15..26.5GHz p1 = 2: 26.5..40GHz p2: [0..255]	Overwriting the EEPROM parameter for the frequency-dependent level correction of the first LO in the RAM, updating the DAC settings for the level correction and status output on the display: p1: frequency range of the new level-correction value p2: new value
2.16.26	p1 = 0: level error of the IF gain p1 = 1: level error of LO p2: [0..255]	Overwriting the EEPROM parameters for the level correction with external mixing in the RAM, updating the system data for the level correction and status output on the display: p1: selection of parameter p2: new value

Function	Parameter	Function description
MW YIG Filter 2.17.x		**MW YIG Filter**
2.17.0		Deletion of all active service functions on this board
2.17.1		-
2.17.2		-
2.17.3	p1 = 0: readout of the EEPROMS p1 = 1: programming of the EEPROMs	This function enables reading the EEPROMs of the MW YIG filter into the MW_YIG.DAT file of the file system (CAL Group) or loading new data from this file into the EEPROMs.
2.17.4	p1: value[0..2] p2: value[0..99]	This function allows for modifying various entries of the EEPROM header block of the board. p1 = 0: type of board, p1 = 1: main modification index p1 = 2: temporary modification index p2 new value for the entry
2.17.5	-	This function programs all data from the EEPROM buffer in the RAM into the EEPROM of the respective board.
2.17.6	p1: bus address p2: subaddress	This function reads out the latest bit pattern which has been programmed into the control register of this board from the RAM copy of the hardware setting and displays it.
2.17.7	p1: bit pattern of mask p2: bit pattern of new value	This function writes the bitpattern transferred in parameter 2 into the register selected by function 2.17.6 at the bit positions given via the mask in parameter 1. The bits thus marked are subsequently disabled for system access.
2.17.8	-	This function reenables system access to the register selected by 2.17.6.
2.17.20	p1:[0..620/800/1340]	Reading out a level correction value from the level correction list for 22/26.5/40GHz of the EEPROM buffer in the RAM and output on the display: p1: address of the correction value to be read out
2.17.21	p1: [0..620/800/1340] p2: [0..255]	Overwriting a level correction value in the level-correction list for 22/26.5/40GHz in the EEPROM buffer in the RAM, updating the interpolation lists for the level correction and status output on the display: p1: address of the EEPROM parameter to be overwritten p2: new value

Function	Parameter	Function description
Detector 2.20.xx		**Detector board**
2.20.0		Deletion of all active service functions on this board
2.20.1	Number of the multiplexer channel to be read out	cyclical readout of the analog-multiplexer channel. Repeating the entry of the same channel terminates the readout for this channel.
2.20.2		-
2.20.3	p1 = 0: readout of the EEPROMS p1 = 1: programming of the EEPROMs	This function enables reading the EEPROMs of the detector board into the DETECTOR.DAT file of the file system (CAL group) or loading new data from this file into the EEPROMs.
2.20.4	p1: Value[0..2] p2: Value[0..99]	This function allows for modifying various parameters of the EEPROM header block of the board. p1 = 0: type of board, p1 = 1: main modification index p1 = 2: temporary modification index p2 new value for the entry
2.20.5	-	This function programs all data from the EEPROM buffer in the RAM into the EEPROM of the respective board.
2.20.6	p1: bus address p2: subaddress	This function reads out the latest bit pattern which has been programmed into the control register of this board from the RAM copy of the hardware setting and displays it.
2.20.7	p1: bit pattern of mask p2: bit pattern of new value	This function writes the bitpattern transferred in parameter 2 into the register selected by function 2.20.6 at the bit positions given via the mask in parameter 1. The bits thus marked are subsequently disabled for system access
2.20.8	-	This function reenables system access to the register selected by 2.20.6.
2.20.20.p1	p1: value (-5V...+5V) in steps of [10mV]. e.g., 1.4V => p1 = 140	This function allows for modifiying the D/A converter for the comparator setting with external trigger.

Function	Parameter	Function description
RF Attenuator 2.21.xx		**RF Attenuator**
2.21.0		Deletion of all active service functions on this board
2.21.1	Number of the multiplexer channel to be read out	cyclical readout of the analog-multiplexer channel. Repeating the entry of the same channel terminates the readout for this channel.
2.21.2		-
2.21.3	p1 = 0: readout of the EEPROMS p1 = 1: programming of the EEPROMs	This function enables reading the EEPROMs of the RF attenuator into the RF_ATT.DAT file of the file system (CAL Group) or loading new data from this file into the EEPROMs.
2.21.4	p1: value[0..2] p2: value[0..99]	This function allows for modifying various parameters of the EEPROM header block of the board. p1 = 0: type of board, p1 = 1: main modification index p1 = 2: temporary modification index p2 new value for the entry
2.21.5	-	This function programs all data from the EEPROM buffer in the RAM into the EEPROM of the respective board.
2.21.6	p1: bus address p2: subaddress	This function reads out the latest bit pattern which has been programmed into the control register of this board from the RAM copy of the hardware setting and displays it. .
2.21.7	p1: bit pattern of mask p2: bit pattern of new value	This function writes the bitpattern transferred in parameter 2 into the register selected by function 2.21.6 at the bit positions given via the mask in parameter 1. The bits thus marked are subsequently disabled for system access.
2.21.8	-	This function reenables system access to the register selected by 2.21.6.

Function	Parameter	Functionsbeschreibung
Dig. IF Board 2.23.xx		**Dig. IF Board**
2.23.0		Deletion of all active service functions on this board
2.23.1	Number of the multiplexer channel to be read out	cyclical readout of the analog-multiplexer channel. Repeating the entry of the same channel terminates the readout for this channel.
2.23.2	-	cyclical output of the status register of the board.
2.23.3	p1 = 0: readout of the EEPROMS p1 = 1: programming of the EEPROMs	This function enables reading the EEPROMs of the digital IF board into the DIGIT_IF.DAT file of the file system (CAL group) or loading new data from this file into the EEPROMs.
2.23.4	p1: value[0..2] p2: value[0..99]	This function allows for modifying various parameters of the EEPROM header block of the board. p1 = 0: type of board, p1 = 1: main modification index p1 = 2: temporary modification index p2 new value for the entry
2.23.5	-	This function programs all data from the EEPROM buffer in the RAM into the EEPROM of the respective board.
2.23.6	p1: bus address p2: subaddress	This function reads out the latest bit pattern which has been programmed into the control register of this board from the RAM copy of the hardware setting and displays it.
2.23.7	p1: bit pattern of mask p2: bit pattern of new value	This function writes the bitpattern transferred in parameter 2 into the register selected by function 2.23.6 at the bit positions given via the mask in parameter 1. The bits thus marked are subsequently disabled for system access.
2.23.8	-	This function reenables system access to the register selected by 2.23.6.

Function	Parameter	Function description
IF-Filter 2.26.xx		**IF Filter board**
2.26.0		Deletion of all active service functions on this board
2.26.1	Number of the multiplexer channel to be read out	cyclical readout of the analog-multiplexer channel. Repeating the entry of the same channel terminates the readout for this channel.
2.26.3	p1 = 0: readout of the EEPROMS p1 = 1: programming of the EEPROMs	This function enables reading the EEPROMs of the IF filter board into the IF_FILT.DAT file of the file system (CAL Group) or loading new data from this file into the EEPROMs
2.26.4	p1: value[0..2] p2: value[0..99]	This function allows for modifying various parameters of the EEPROM header block of the board. p1 = 0: type of board, p1 = 1: main modification index p1 = 2: temporary modification index p2 new value for the entry
2.26.5	-	This function programs all data from the EEPROM buffer in the RAM into the EEPROM of the respective board.
2.26.6	p1: bus address p2: subaddress	This function reads out the latest bit pattern which has been programmed into the control register of this board from the RAM copy of the hardware setting and displays it.
2.26.7	p1: bit pattern of mask p2: bit pattern of new value	This function writes the bitpattern transferred in parameter 2 into the register selected by function 2.26.6 at the bit positions given via the mask in parameter 1. The bits thus marked are subsequently disabled for system access.
2.26.8	-	This function reenables system access to the register selected by 2.26.6.
2.26.20	CalAmp1-value as integer: -3 .. +12 [dB]	The gain factor entered via parameter 1 is set for CalAmp1 and protected against system access. System access is enabled again by means of the function 2.26.0. The gain factor is then overwritten prior to the next sweep by the currently used gain.
2.26.21	CalAmp2-value as integer: -6 .. +9 [dB]	The gain factor entered via parameter 1 is set for CalAmp2 and protected against system access. System access is enabled again by means of the function 2.26.0. The gain factor is then overwritten prior to the next sweep by the currently used gain.

6.3 Test Instruments and Utilities

Item	Type of Instrument	Required specifications	Suitable R&S Instrument	Order No.	Application
1	Digital multimeter	1mV...100V 0.1mA...1A	UDS5	349.1510.02	
2	Frequency counter	Accuracy >1*10^{-8}			
3	Signal generator	100kHz...3500MHz	SMHU	835.8011	
4	3-dB coupler	Decoupling >20dB; 1 to 3500MHz			
5	Attenuator	6dB	DNF	274.4110.50	
6	Spectrum analyzer	100kHz to 8000MHz	FSM	1020.7020.52	
7	Power meter	100kHz to 3500MHz	URV5 NRV-Z?	349.8012.02	
8	Network analyzer	300kHz to 3500MHz			
9	VSWR bridge	300kHz to 3500MHz			

6.4 Troubleshooting

3 selftest functions are available to ease troubleshooting:
The user selftest described in Section 4 is appropriate for determining on which board the error occurred.
The service selftest described in Section 6.1.4.3 supplies additional information on the error by output of the faulty test functions.
When the automatic test has been performed the individual circuitry on a board can be checked by calling the board tests. After calling the test functions, the current tolerance limits of the test voltage are displayed, thus allowing to obtain further information on the faulty functions of the board.
The following sections are intended to support troubleshooting assuming various error symptoms by way of example.

6.4.1 No Reaction or Faulty Reaction upon Switch-on

- The SUPPLY-CHECK LED on the power supply lights up with power switch and on-switch switched on.
- Check operating voltages on the motherboard:
  X190 A 6 +5.2V ±0.2V
  X190 A 29 -15V±0.2V
  X190 A 30 +15V ±0.2V
  X190 A 31 +5.5V±0.2V

- Problems which occur with booting the transputer net may be due to a missing clock signal. Operation of the level transputer on the detector board requires 20 MHz which are supplied by the fracsyn.
  Measurement : X145 20 MHz TTL

- If no TTL signal is applied to X145 an, check at X144, whether the reference oscillator oscillates with 120 MHz:
  Measurement: X144 120 MHz >8 dBm

6.4.2 Error Messages During Operation

Even with normal operation, the controller monitors the functions which are important for operation of the instrument such as the lock-in indications for the synthesizer loops (LO unlock message), the level detectors for the LO signals at the mixers (Level LO message) and overranging in the signal path.
Starting the selftest (comp. Section 6.1.3.3) should localize the error source as far as possible. Since, however, the selftest of the instrument is limited, the following messages, which are arranged according to the error messages, should be performed prior to replacing the module which is assumed to be defective.

6.4.2.1 Error Message: 1st LO unlock

The first LO has been realized in the FSE by a YIG oscillator, which is synchronized to the output signal fo the "FRACSYN" module. Refer to Section 6.1.2.7 for a description of the module function and the illustration in a block diagram.

Causes for unlocking of the first LO:

- faulty adjustment of the YIG-oscillator pretuning or pretuning faulty
- level with sampling signal too low or signal on the wrong frequency
- sampling mixer faulty
- YIG oscillator faulty
- FM-coil driver for YIG oscillator faulty

If the error occurs only temporarily, e.g., with warming up of the instrument or with high / low temperatures, an adjustment of the motherboard of the RF module should be performed first to exclude effects due to ageing of components. The adjustment is explained in the description of the RF modules.

Appearance of the above-mentioned errors in the instrument

Total failure of the YIG synchronization
If one of the above-mentioned errors occurs in the instrument, the subsequent setting leads to an appearance similar to that shown in the figure below.

Setting on FSE :
- reset
- center 120 MHz
- span 200 MHz
- switch input to calibration signal
- switch on selftest voltage for YIG loop
  using service function 2.xxxxxxx

Fig. 6.1 Appearance with main loop unlocked, when the sampling signal is missing. The frequency offset is approx. 50 MHz, then.

Fig. 6.2 Representation of the calibration signal with a span of 50 MHz. If the synchronization is missing, the stepping of the YIG pretuning is visible.

The following thorough error analysis requires the indicated frequency offset:
measurement marker -> peak, frequency offset = marker frequency - 120MHz

When synchronization is missing, the YIG oscillator is only swept at the relatively rough stepping of the pretuning, i.e., approx. 1 MHz with FSEA, approx. 2 MHz with FSEB and FSEM. This causes clearly visible steps to occur on the display, if the span is selected accordingly small. With spans <= 30 MHz the pretuning value is held. Thus, the signal is not displayed with failure of the PLL. The error can then be concluded from the selftest voltage and the displayed frequency offset.

Error causes

Frequency offset < 10 MHz
If the measured frequency offset is below 10 MHz with the above setting, the connection between the FRACSYN module and the fine tuning of the YIG oscillator is presumably interrupted. This is either due to a defective connecting cable between X149 and X139 or to a faulty FM-coil driver on the RF module. A closer examination is to be carried out according to the description of the RF module.

Frequency offset between 40 and 60 MHz
If the selftest voltage is more negative than the permitted voltage and the frequency offset of the signal is between +40 and +60 MHz with the above setting, or if the selftest voltage is at the positive stop and

the frequency offset is between -40 and -60 MHz, the error is located in the signal conditioning of the YIG-oscillator control loop and may be due to the following reasons:

- no signal at the output X142 of the FRACSYN module
- incorrect frequency at the output X142
- cable from X142 to YIG sampler disconnected (X133)
- YIG sampler faulty, i.e., no mixed signal at X134
- cable from X134 to X143 disconnected
- phase detector on FRACSYN defective

The output signal of the FRACSYN at X142 is checked by the selftest with regard to level and frequency, see Section 7.3.5 Troubleshooting FRACSYN, an additional measurement can be performed using the following settings. The same applies for the output signal of the YIG sampler, the level of which is checked at the input X143 of the FRACSYN.

Setting: reset; span 100MHz; single sweep

For signal measurement with maximum and minimum frequency, the center frequency has to be set, accordingly. A single sweep has to be performed following each setting in order to make sure that the FSE accepts the value!

Measurement of interpolation synthesizer:
Connect spectrum analyzer to X142

Measured value:
with FSEA and center frequency 50 MHz : 491.2666 MHz, >10dBm
with FSEA and center frequency 1790 MHz : 684.6 MHz, >10dBm

with FSEB / M and center frequency 50 MHz : 503.2125 MHz, >10dBm
with FSEB / M and center frequency 6950 MHz : 679.609 MHz, >10dBm

Harmonic suppression > 12dBc; frequency deviation below 1ppm

Considerable deviations indicate that the FRACSYN module is probably faulty, proceed as explained in the board description. If the LO Phase module is fitted, the same measurement must be repeated at the connector X123 of the LO Phase. The measurement values must adhere to the same limits. If deviations occur, proceed as explained in the description of the LO Phase.

Testing the output signal of the YIG sampler

Disconnect the connection between X139 and X149, shortcircuit board input X139 on the RF module to ground.
If the frequency offset adhered to the given tolerance with the previous FSE settings, a 30-MHz signal +-20 MHz with a level >= -25dBm should be applied to the connector X133. For this measurement, repeat the two settings of the previous measurement. If the YIG loop unlocks with particular frequencies only, check whether the output level at the sampler is sufficient with these frequencies.
This check requires that the FRACSYN signal (at X 132) is applied with the correct level and frequency and that the YIG is correctly tuned. Both requirements should be met by the preceding tests.
If the level of the output signal of the sampler is below the indicated limit, the YIG sampler is faulty. In this case a replacement module can be obtained and replaced. The motherboard of the RF module must then be readjusted according to the board description. Adjustment is not required if the complete module is replaced.

No signal or offset exceeding +- 60 MHz

In this case, either a YIG oscillator or the pretuning is faulty. Since the YIG can only be replaced together with the YIG sampler on the RF module, the pretuning should be checked by an additional measurement to save costs.

Testing the YIG coarse tuning

Disconnect the connection from X149 to X139 and connect the input of the RF module (X139) to ground. Then perform the subsequent measurements:

Setting on FSE: reset; span 0; center frequency according to table
Measurement: connect spectrum analyzer at X... directly to the YIG sampler on the RF module

Measured value:

	Center frequency	Frequency / MHz	Level / dBm	Voltage X130 A17
FSEA	0 Hz	4341.4 +- 20	> -20	1.391 V +- 10 mV
	3.5 GHz	7841.4 +- 20	> -20	9.627 V +- 10 mV
FSEB/ FSEM	0 Hz	7941.4 +- 40	> -10	0.519 V +- 10 mV
	7GHz	14941.4 +-40	> -10	8.755 V +- 10 mV

The voltage at X130 pin A17 is supplied by the FRACSYN module and provides for the pretuning of the YIG oscillator. If this voltage is already out of tolerance, the oscillator frequency does not adhere to the above-mentioned values either. Open the line at the board adapter to check whether the voltage is supplied incorrectly by the FRACSYN module or if the board is loaded excessively by the RF module (e.g., by a defective main-coil driver, which initiates the YIG pretuning). If the voltage applied at the output of the FRACSYN module is correct subsequent to opening the line, the motherboard of the RF module should be checked and replaced, if required. A replacement of the motherboard requires adjustment of the module. If the voltage at the output of FRACSYN remains to be incorrect, the error is located in the FRACSYN module. Repair of the module is not advisable since it is a very complex digital circuit. The board should rather be replaced by a spare board.
If the measured frequency approximates or exceeds the above-mentioned deviation, the motherboard of the RF module should be adjusted. The adjustment instruction is contained in the board description.
If the levels deviate considerably from the rated values, the fault is located in the YIG sampler or its voltage supply. Further troubleshooting requires connection of the board via an adapter cable and voltage check at the feedthrough filters on the solder side of the main board according to the board description. The milled housing of the YIG sampler contains very sensitive microwave circuits which is why it must not be opened! With failure of the sampler, a spare module can be obtained, however, the main board must be readjusted. The adjustment is performed according to the board description.

Faulty adjustment of RF module

A slightly incorrect adjustment of the motherboard of the RF module, as might occur due to ageing, causes the message "1st LO unlock" to occur only with large span and/or little sweep time.

Setting on the FSE :
- reset
- with FSEB / FSEM stop frequency 3.5 GHz
- sweep time 100ms
- apply signal with 1.75 GHz, e.g.

Fig. 6.3 Full span with dynamic faulty adjustment, the signal is displayed depending on the sweep time with incorrect frequency or jittered, as in this example.

In this case, new adjustment of the RF module is required. Refer to the troubleshooting section of the RF-module description for adjustment instructions.

6.4.2.2 Error Message 2nd / 3rd LO unlock

The 2ndIF Converter module is considerably involved in the generation of the second and third LO. In the FSEA, the output signal of the 2ndIF Converter is directly used as second local oscillator, in the FSEB / M, the signal is still doubled in the RF module. The third LO is approx. 720 MHz with all models and is used for conversion of the second to the third IF on the same board, which it is generated on. The third LO is the output signal of an oscillator with small tuning range which can be pulled electronically. This VCO is pulled close to the rated frequency and, in parallel, it is regulated to the sixth harmonic of the 120-MHz reference of the FRACSYN by means of a PLL:
Since the second LO is obtained by multiplication of the third LO, both can be asynchronous to the reference simultaneously only. The frequency offset of a displayed signal is independent of the receive frequency if the 2nd LO is unlocked and is approx. 100kHz to approx. 2MHz.

Setting on the FSE :
- reset
- center 120 MHz
- span 8 MHz
- switching the input to calibration signal

Fig. 6.4 Asynchronous 2nd LO with incorrect pretuning or reference signal being too small. If the 120-MHz reference is missing, the frequency is similarly apart, but the signal shows no secondary lines.

Causes for unlocking of the third LO
- 120-MHz reference from FRACSYN missing
- incorrect data in the EEPROM of the 2nd IF Converter for the VCO pretuning
- PLL or VCO of 2nd IF Converter defective

Measuring the 120-MHz reference
Test utility: spectrum analyzer
Measurement: connect analyzer to the cable to X154
rated level > +8dBm
frequency = 120 MHz +- 1ppm
reconnect cable to X154

Measurement of the 3rd LO
Test utility: spectrum analyzer
Measurement: connect analyzer to X155
rated level > +8dBm
frequency = 720 MHz +- 1ppm

If the signal at X155 is outside the above-mentioned limits, though the 120-MHz signal is correctly applied to X154, the error is located in the 2nd IF Converter which should be further examined using the board description. If the 120-MHz signal at X154 is already missing, an amplifier stage in the FRACSYN could be faulty. If an option is fitted, which requires the 120-MHz frequency, a measurement at the female X144 reveals whether the signal is present there. The connection between X144 and X154 is made via an option board in the option which require the 120-MHz reference and it may be disconnected.

6.4.2.3 Error Message 120-MHz Reference Unlock

The unlock message of the 120-MHz crystal oscillator may be caused by the following facts:

- level too low or frequency offset too large with external reference
- frequency offset of the 120-MHz oscillator too large
- TCXO on the FRACSYN module faulty
- OCXO still cold with LO Phase option fitted or failure inside cable X128
-> X148

- faulty adjustment of TCXO or OCXO

The first three items can be checked using the FRACSYN description. If the TCXO frequency violates the permitted tolerance, it can be readjusted via a DA converter using the service functions. This adjustment is explained in the FRACSYN description, too.

If the LO Phase option is fitted to the FSE, check whether the OCXO is switched on. Measurement of the OCXO operating voltages is explained in the FRACSYN description (section).

If the OCXO operating voltage is outside the tolerance, the FRACSYN module is faulty. If the OCXO does supply any signal at X128 although the operating voltage is provided, the OCXO is faulty. If the OCXO frequency violates the tolerance, it can be readjusted similar to the TCXO using a service function. The instructions for adjustment of the OCXO can be looked up in the section on the FRACSYN module, as well.

6.4.2.4 Error Message: Level LO

This error message is output when a level detector indicates that the signal at the LO gate of a mixer is too small. The FSE calls the selftest to check, which of the detectors indicates the error.

6.4.3 Error Message during Selftest

6.4.4 Error Message with Calibration

If one of the warnings or error messages described in the operating manual occurs with short or total calibration, it is useful, to output the calibration values and check the deviations. If the deviations from the rated values are fairly large, check the board using the respective service instructions.

6.5 Testing and Adjustment

All boards of the FSE have been adjusted before being supplied and do not require readjustment after a board replacement in the instrument.
The correction and setting data for the boards are contained in an EEPROM on each board and are thus replaced with board replacement.

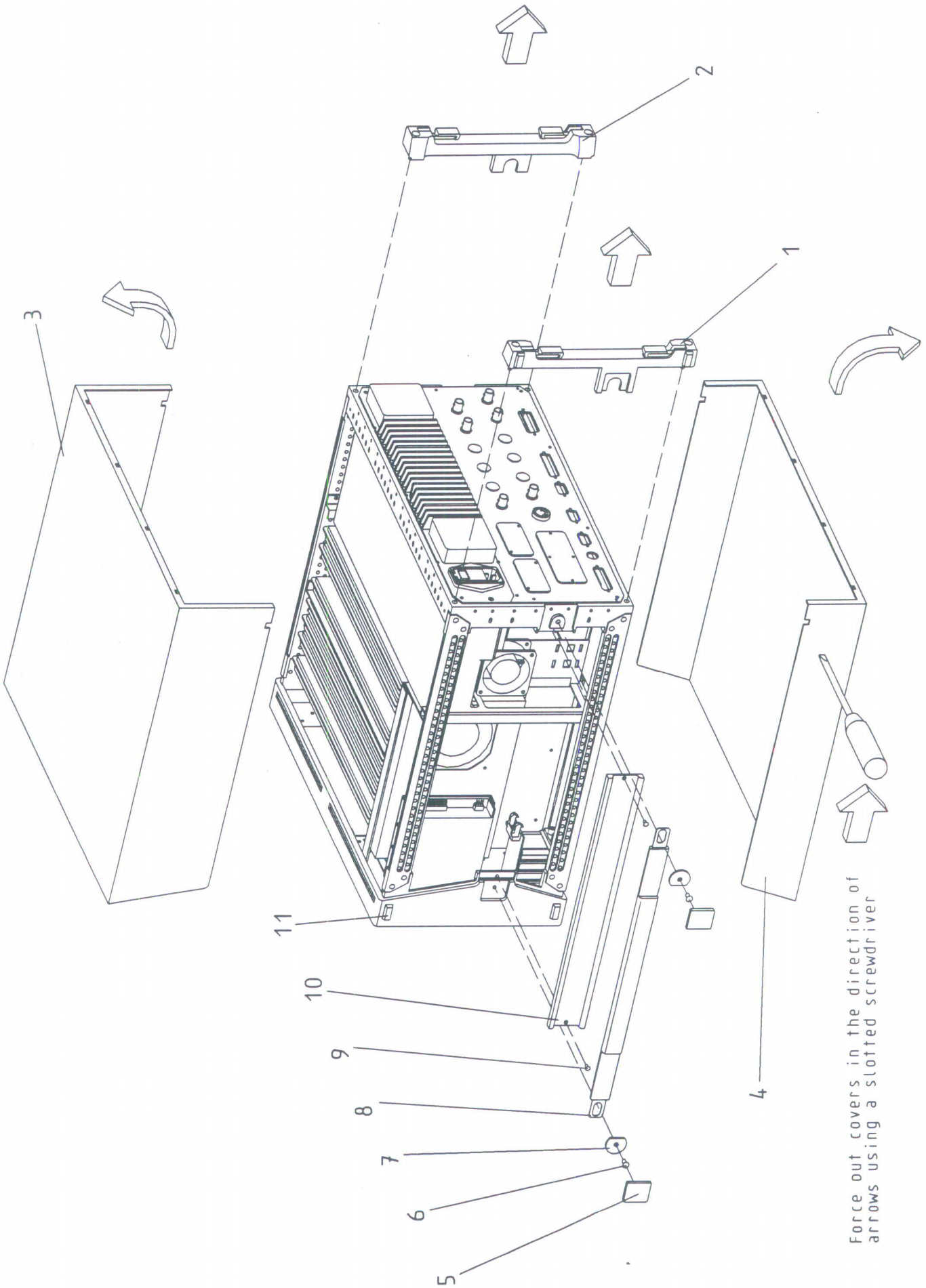
Switch off the instrument before replacing a board.

Some boards provide additional adjustment facilities which should be checked with servicing:

- Fracsyn: adjustment for calibration level -40dBm
- RF-Converter: adjustment of the YIG oscillator characteristic and dynamic
- 2nd IF-Converter: no adjustment
- IF filter: no adjustment, all values are determined with calibration
- Detector: no adjustment
- LowPhaseNoise: no adjustment

Necessary adjustments are described in the section of the respective boards.

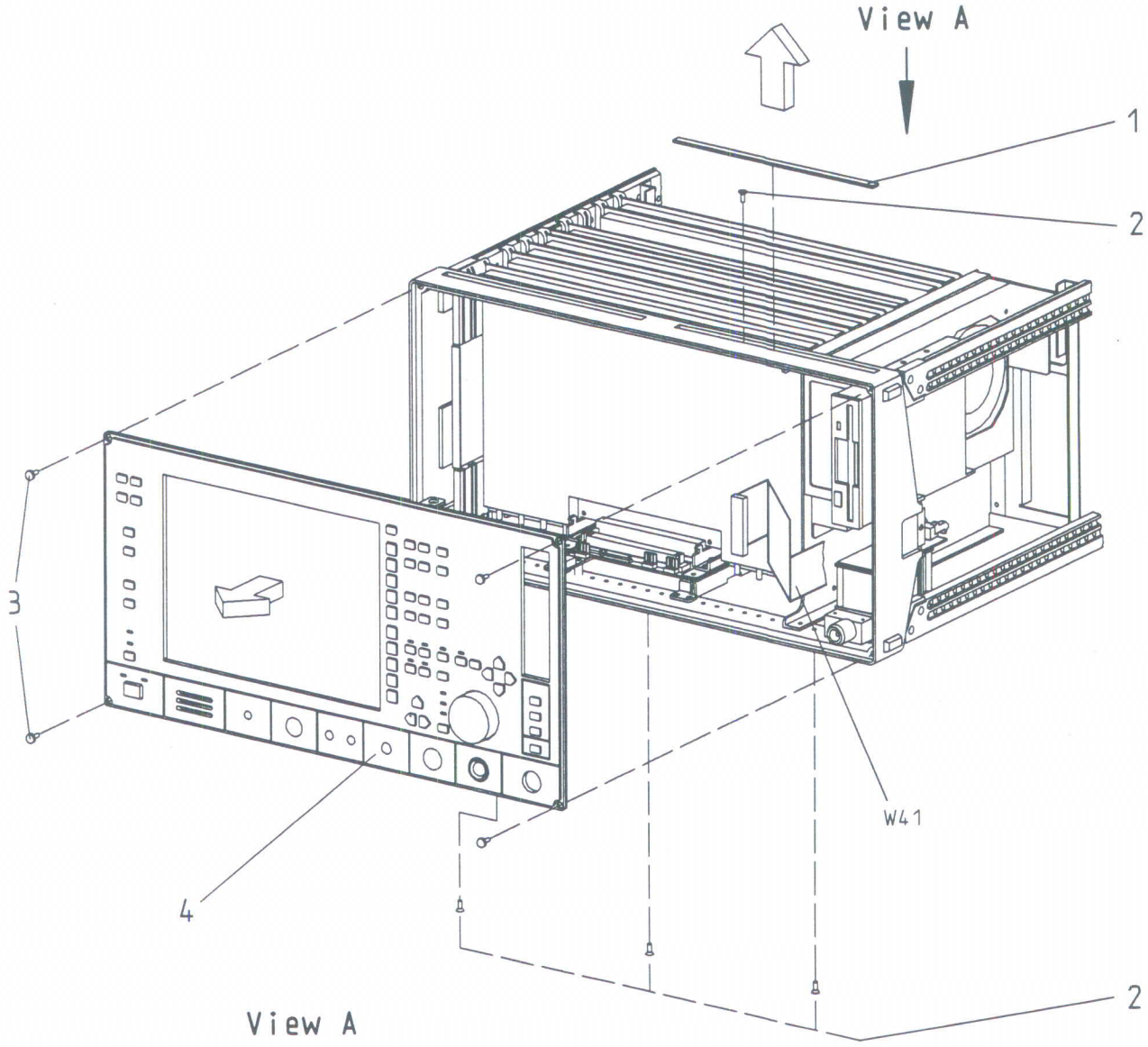
Adjustment of the reference frequency is explained in Section 4.1.2 (Maintenance and Troubleshooting).

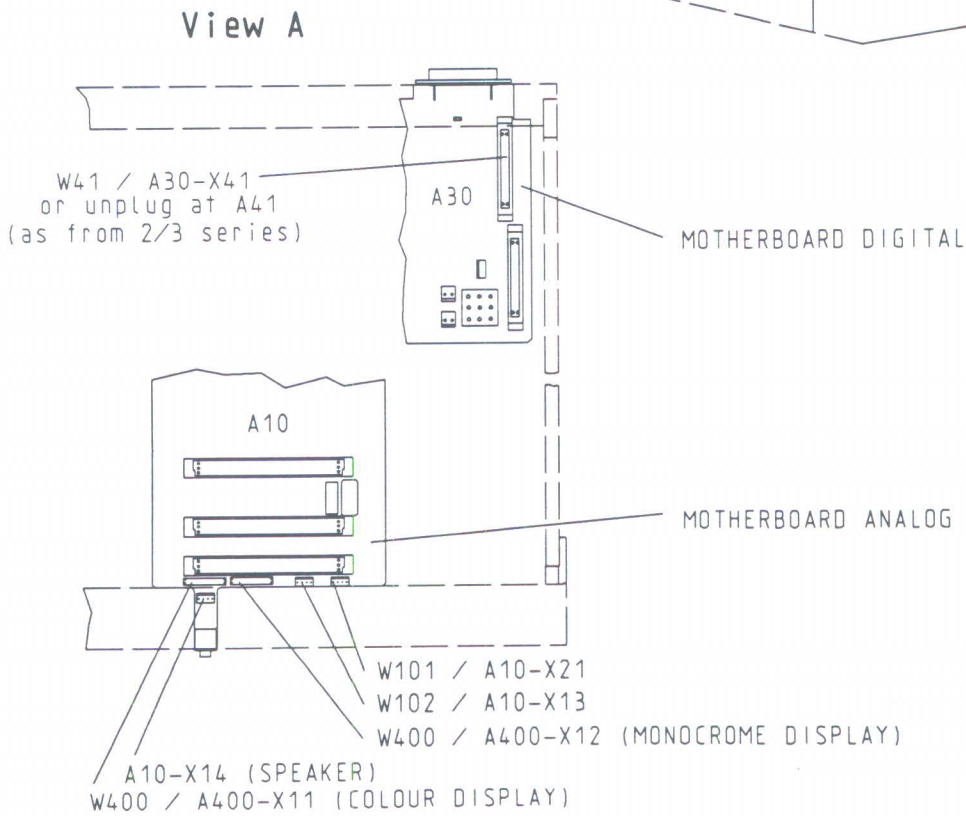

1
2
3
4
5
6
7
8
9
10
11
Force out covers in the direction of arrows using a slotted screwdriver

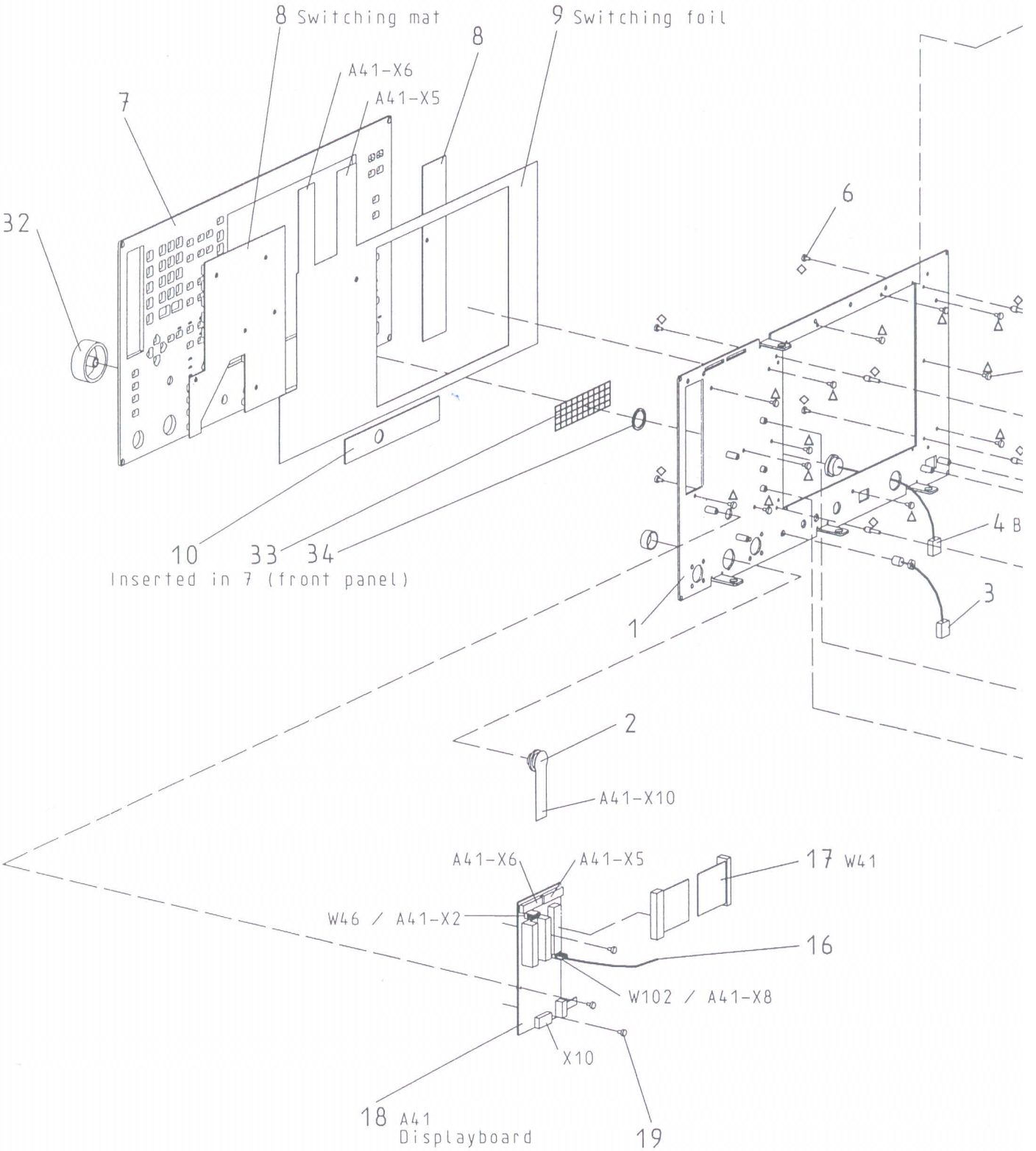
Panelling

Item	Designation	Quantity	Ident. No.
1	Right-hand rear panel foot 5U	1	0396.4186.00
2	Left-hand rear panel foot 5U	1	0396.4392.00
3	Upper cover 5E 1/1 T460	1	1065.9115.00
4	Lower cover 5E 1/1 T460	1	1065.9167.00
5	Cover on handle side	4	0396.3350.00
6	DIN965 M4 x 10	4	0081.9478.00
7	Thread	4	0396.3367.00
8	Handle T460	2	0396.3221.00
9	DIN965 M3 x 6 PA	4	0396.8030.00
10	Side strip T460	2	0396.3080.00
11	Side foot	4	0396.4692.00

6.6.3.1 Front panel FSE (A20)



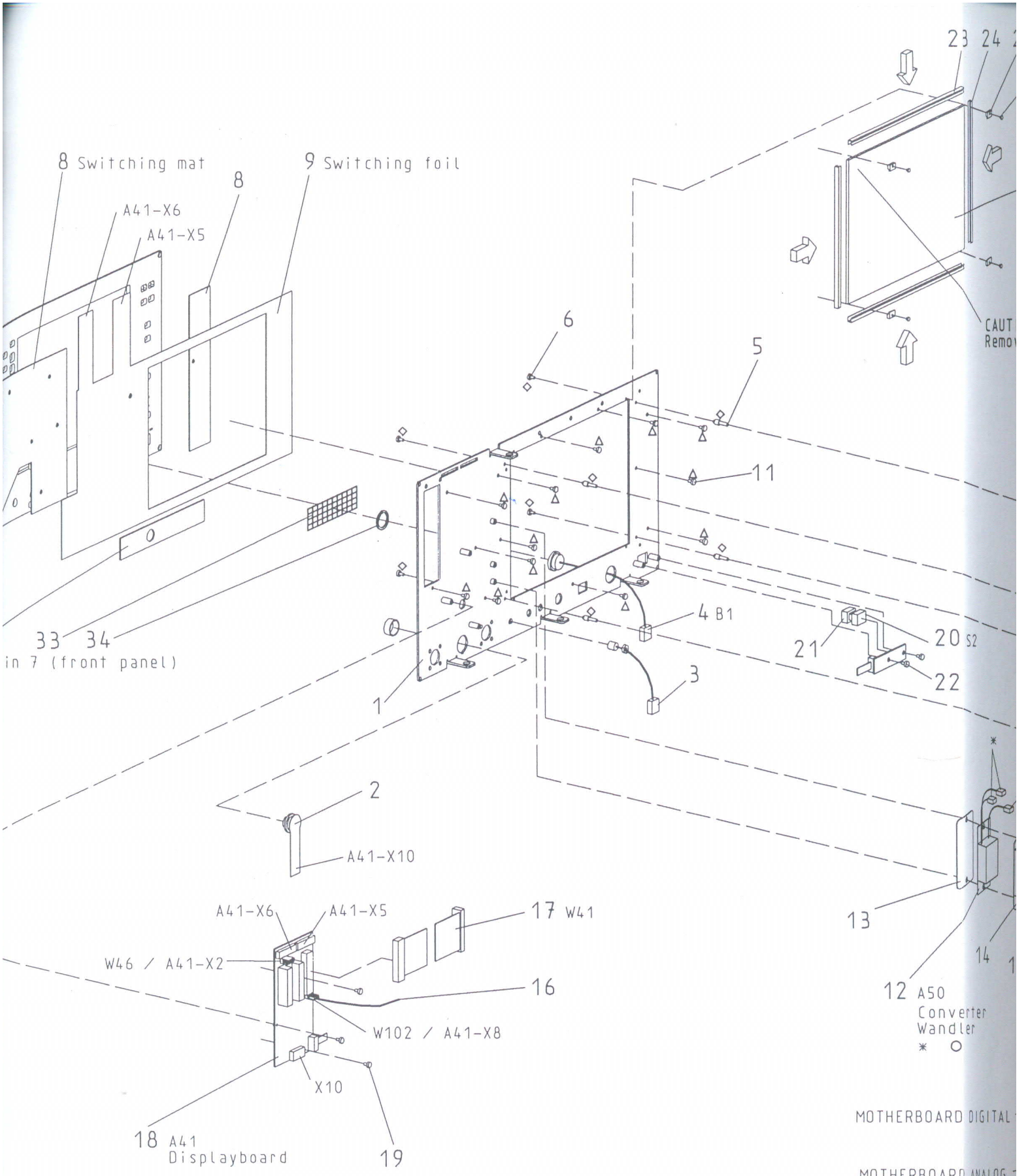




Screws for LCD and switching mat

◇ For item 28 (LCD)

△ For item 8 (switching mat)

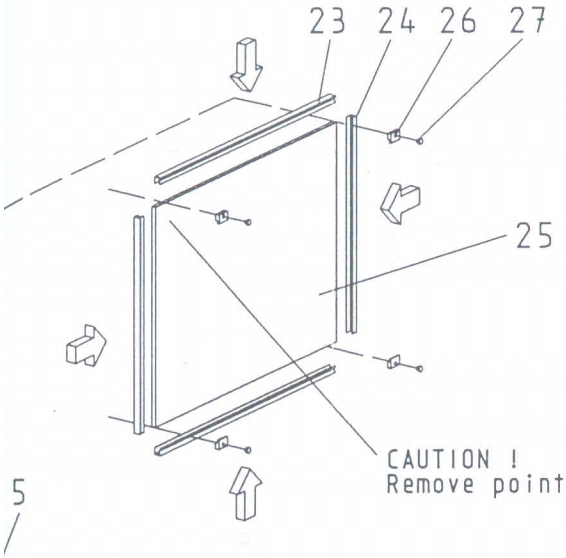


Screws for LCD and switching mat

◇ For item 28 (LCD)

△ For item 8 (switching mat)

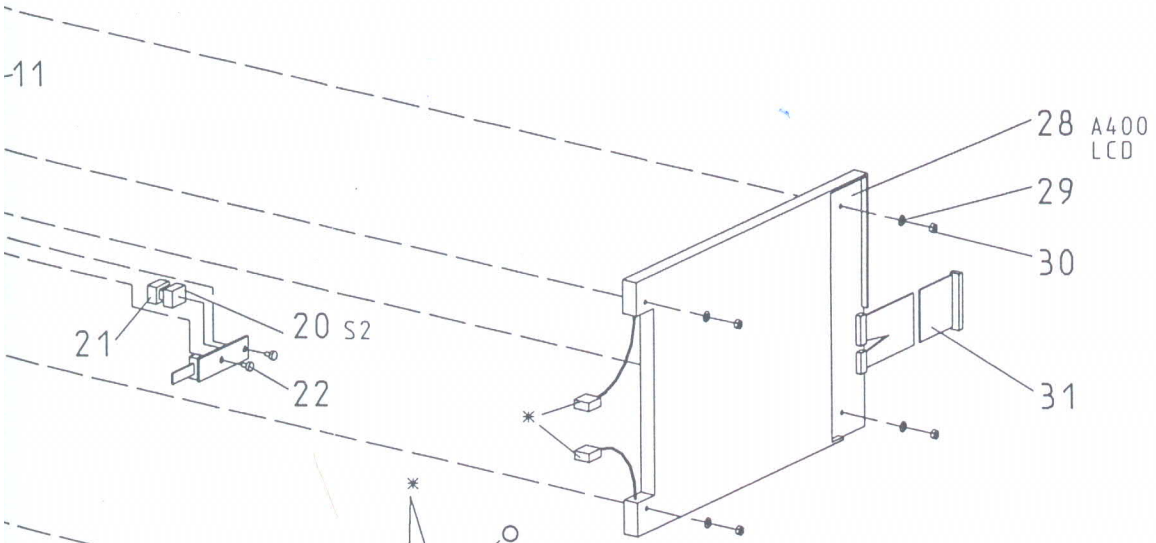
6.6.3.2
Front panel (components)

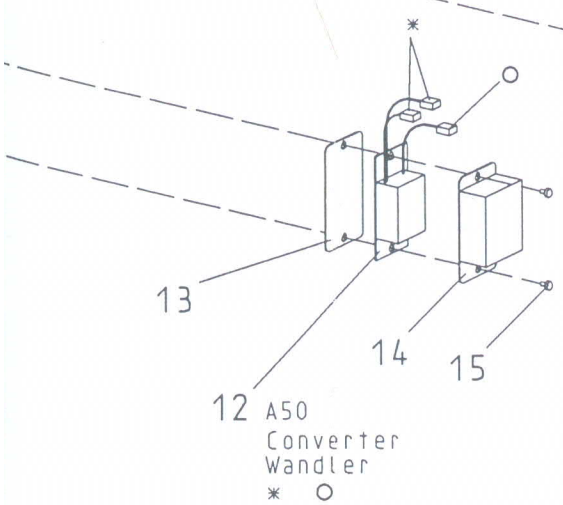


Put 23 and 24 on filter plate, then press into 1 (mounting plate) and screw on together with 26 and 27.

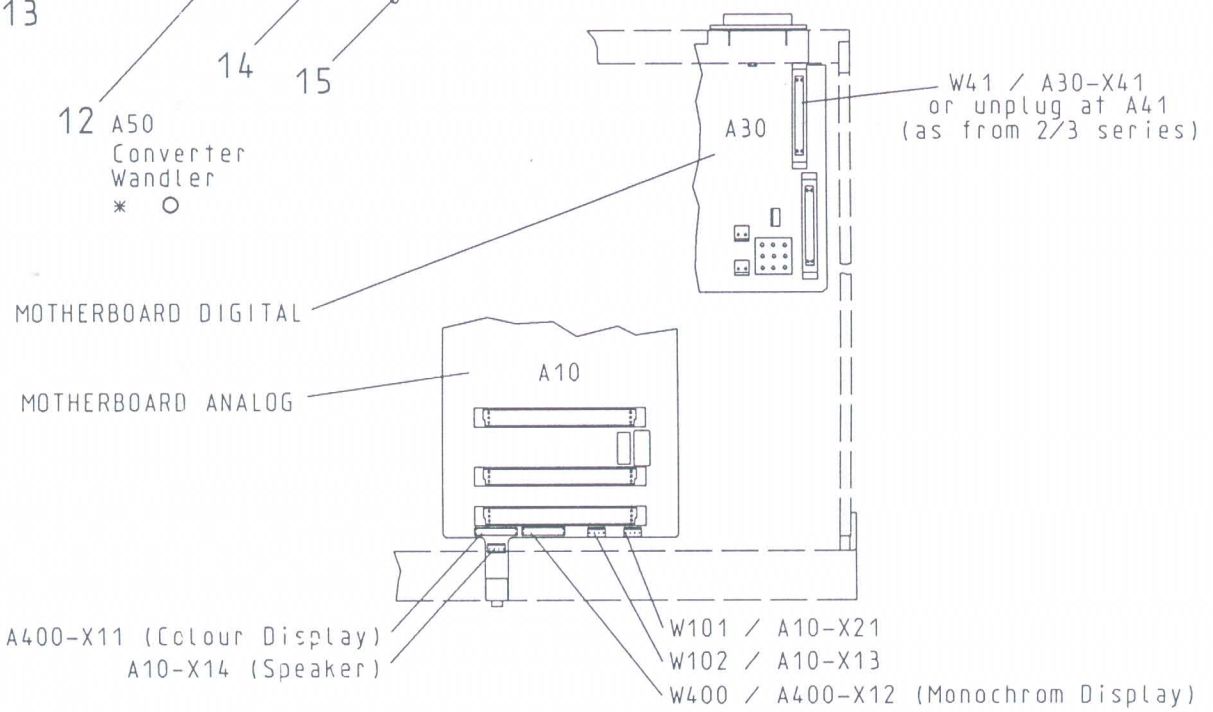
5

-11





* for Colour Display
O for Monochrome Display



Front Panel (A20), Individual Parts

Instructions for disassembly: - Remove panelling according to 6.6.1
- Disassemble complete front panel according to 6.6.3

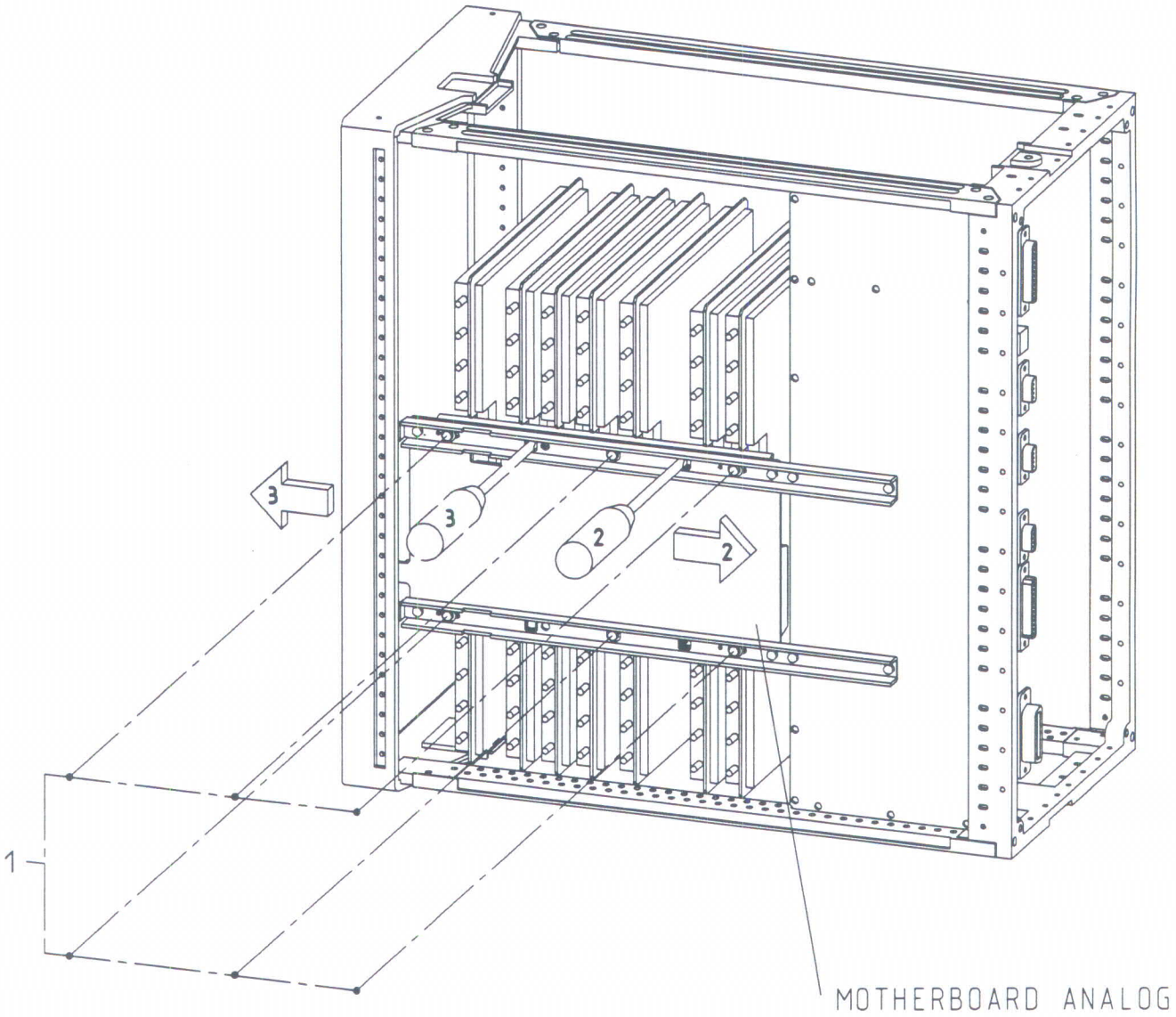
Item	Designation	Quantity	Ident. No.
1	Assembly plate	1	1065.6374.00
2	12-contact female connector	1	1065.8748.00
3	Cable W101	1	1065.9221.00
4	Loudspeaker	1	1065.9215.00
5	Thread pin for VAR02 Thread pin for VAR03	4 4	1065.6380.00 1065.6397.00
6	DIN965 M2.5 x 5 PA	4	0852.3608.00
7	Printed front panel	1	1065.6280.00
8	70-key switching mat	1	1065.6316.00
9	71-key switching foil	1	1065.6345.00
10	FSE strip	1	0852.1740.00
11	Screw for plastics plate	12	0852.3250.00
12	* Converter board for VAR02 O Converter board for VAR03	1 1	1043.1070.02 1043.1070.04
13	Cover	1	1043.1034.00
14	Hood	1	1043.1028.00
15	Screw with washer assembly M2.5 x 6	4	0071.5040.00
16	Cable W102	1	1065.9238.00
17	Cable W41	1	1065.7787.00
18	Display board (A41)	1	1065.7764.02

19	Screw with washer assembly M2.5 x 6	3	0071.5040.00

Item	Designation	Quantity	Ident. No.
20	Key without button (S2)	1	0821.8389.00
21	Key cap	1	0396.0145.00
22	Screw with washer assembly M2.5 x 5	2	0071.6830.00
23	RF spring (201)	2	1069.3034.00
24	RF spring (153)	2	1069.3040.00
25	FSE filter plate	1	1069.2015.00
26	Plate holder	4	0852.0844.00
27	DIN965 M2 x 4 PA	4	0852.3508.00
28	Colour LCD VAR02 (A400) Black/white LCD VAR03 (A400)	1 1	0009.7714.00 0009.7150.00
29	DIN125 A3,2-A4	4	0082.4670.00
30	DIN934 M3	4	0016.4398.00
31	34-contact cable VAR02 17-contact cable VAR03	1 1	1065.8883.00 1065.8783.00
32	Rotating knob RD37	1	0852.1057.00
33	Grid	1	1065.6268.00
34	Ring	1	1065.6351.00

6.6.4 Analog section (without own drawing)

6.6.4.1 Locking / Unlocking Analog Modules

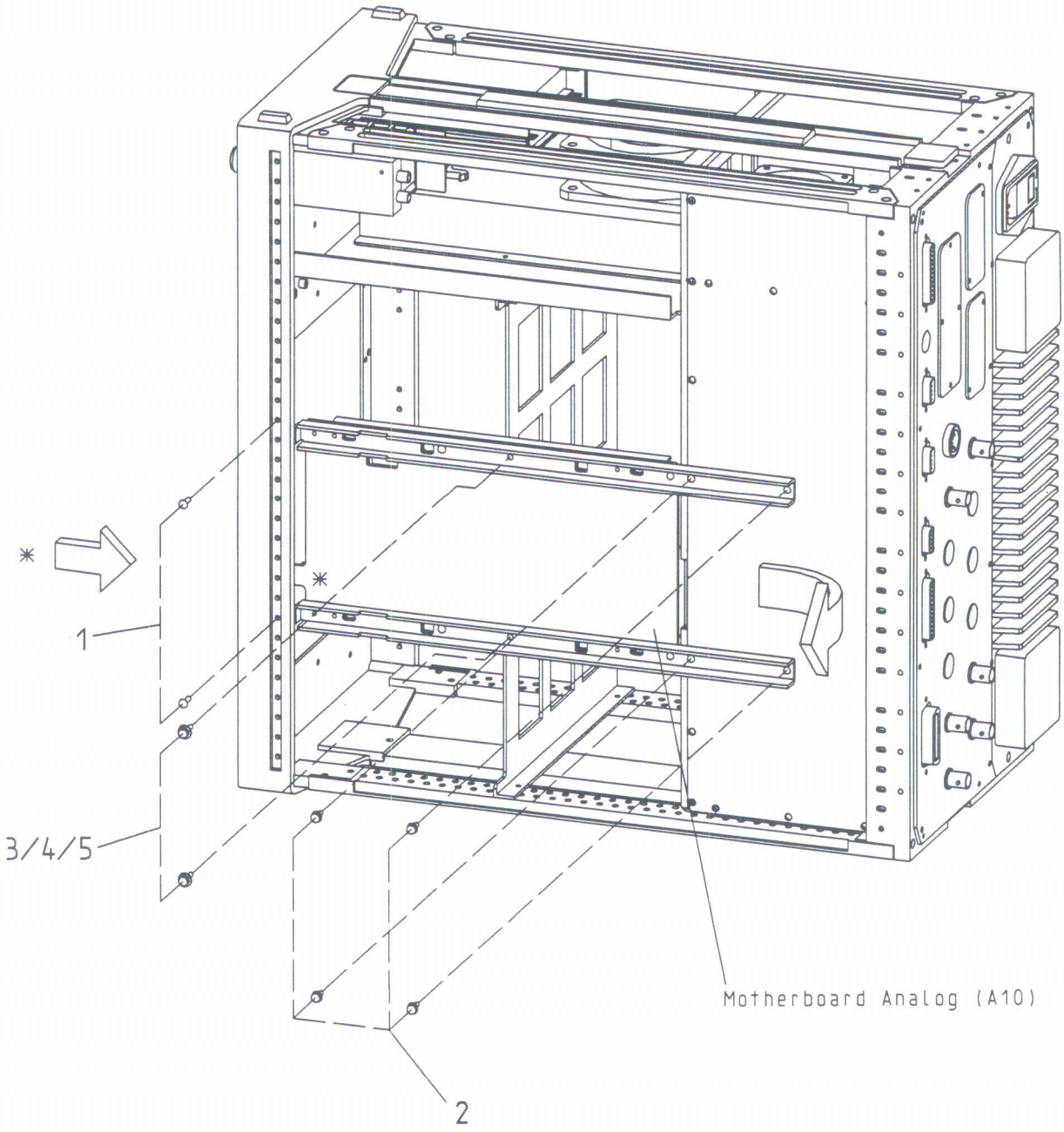


1 = Loosen screws (6x)

2 = Loosen interlock circuit

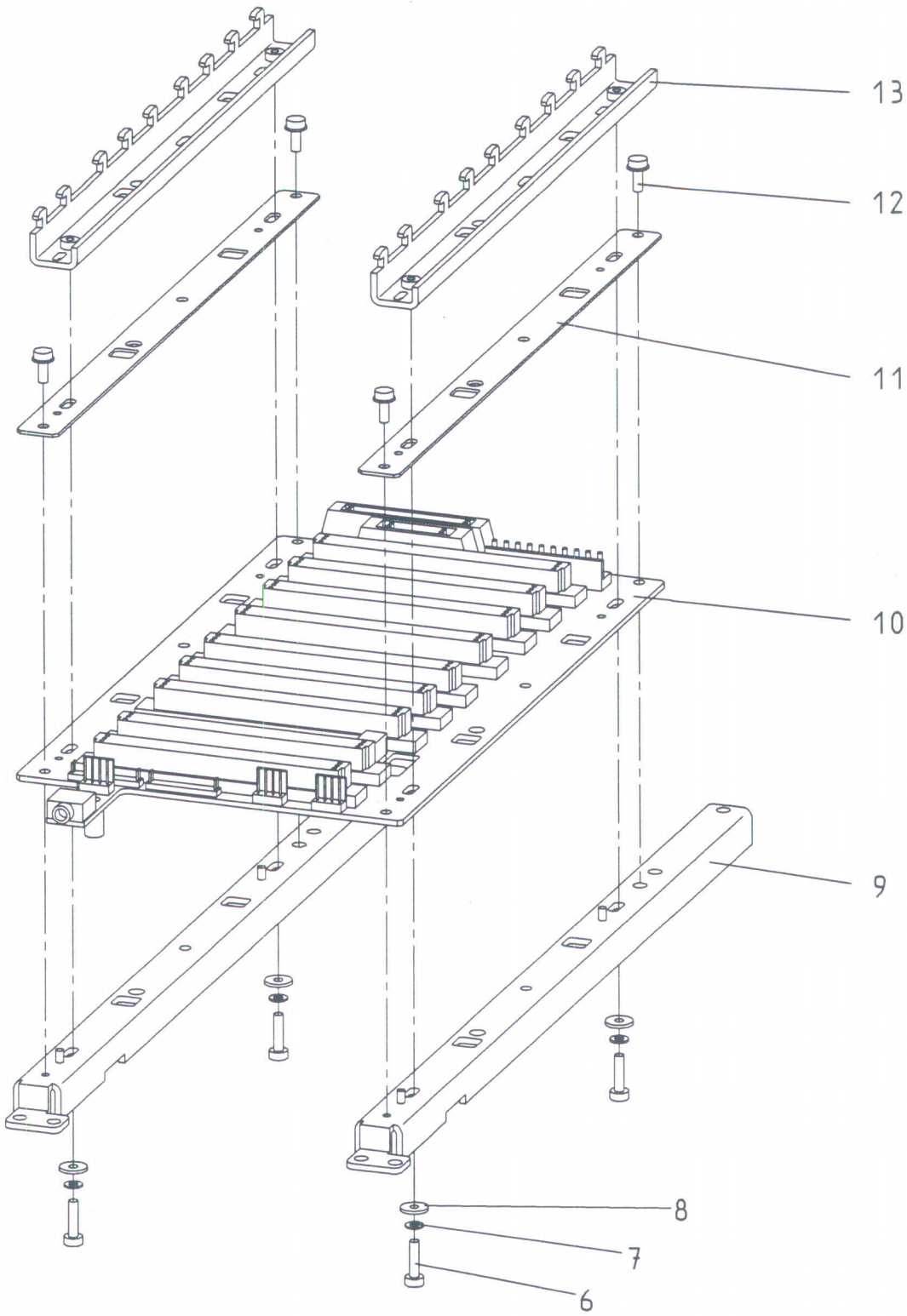
3 = Lock circuits and tighten screws (1) (6x)

6.6.4.2 Motherboard Analog (A10)



***CAUTION:** take care not to damage loudspeaker female connector (front panel) on removing the motherboard

6.6.4.2 Motherboard Analog (A10)



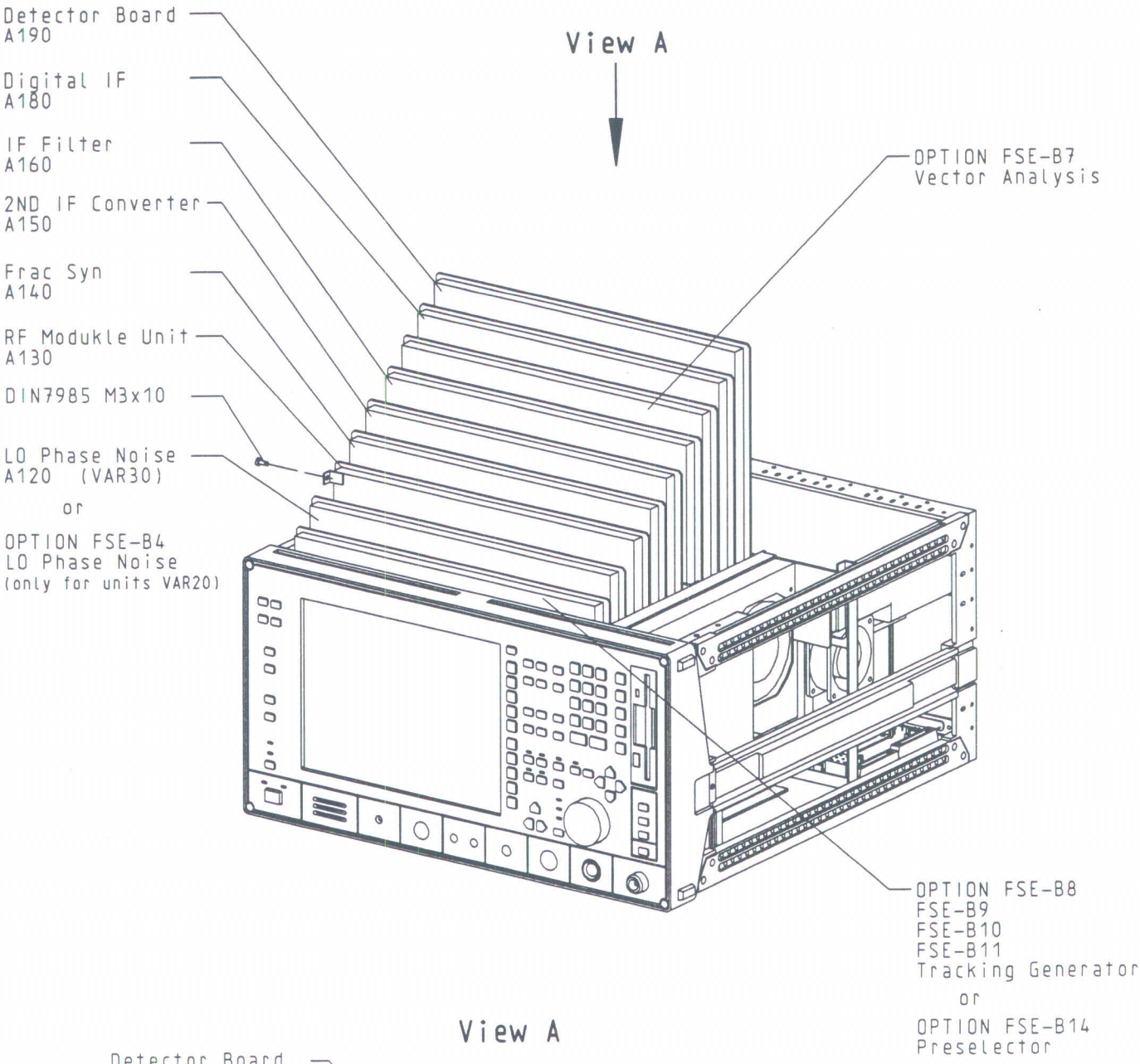
Motherboard Analog (A10)

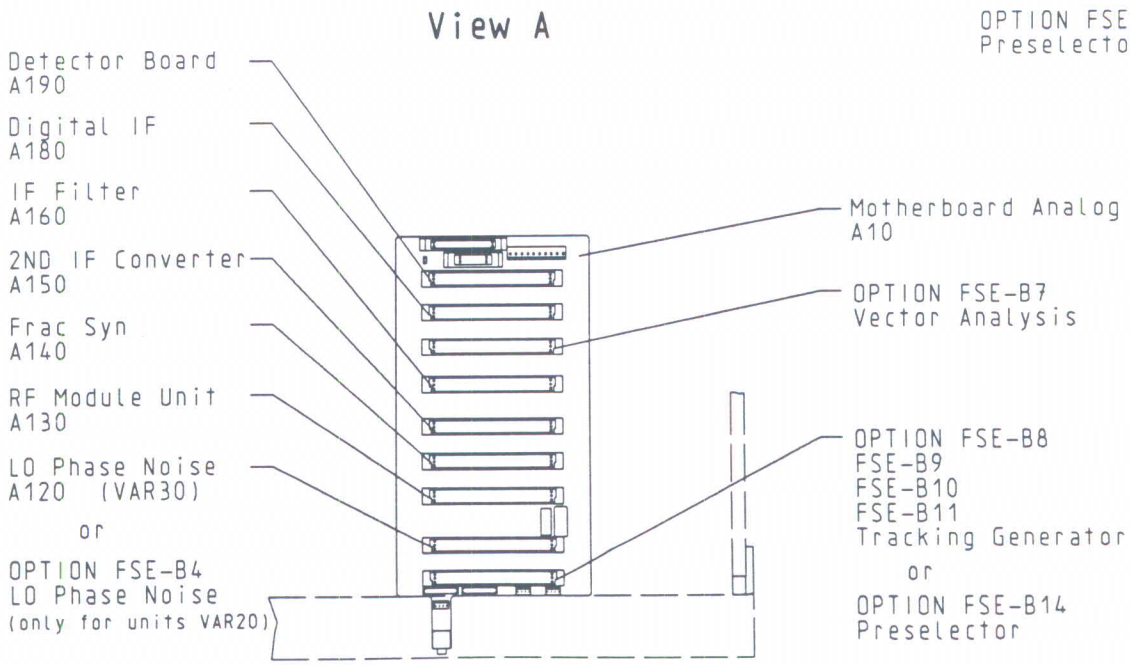
Instructions for disassembly:
- Remove panelling according to 6.6.1
- Loosen cabling from analog modules
- Unlock analog modules on A10 (see 6.6.4.1)
- Disassemble all analog modules
- Unplug all cables from motherboard (eg front panel)
- Disassemble in the sequence given in the table

Caution: Take care not to damage loudspeaker female connector (front panel) on removing the motherboard

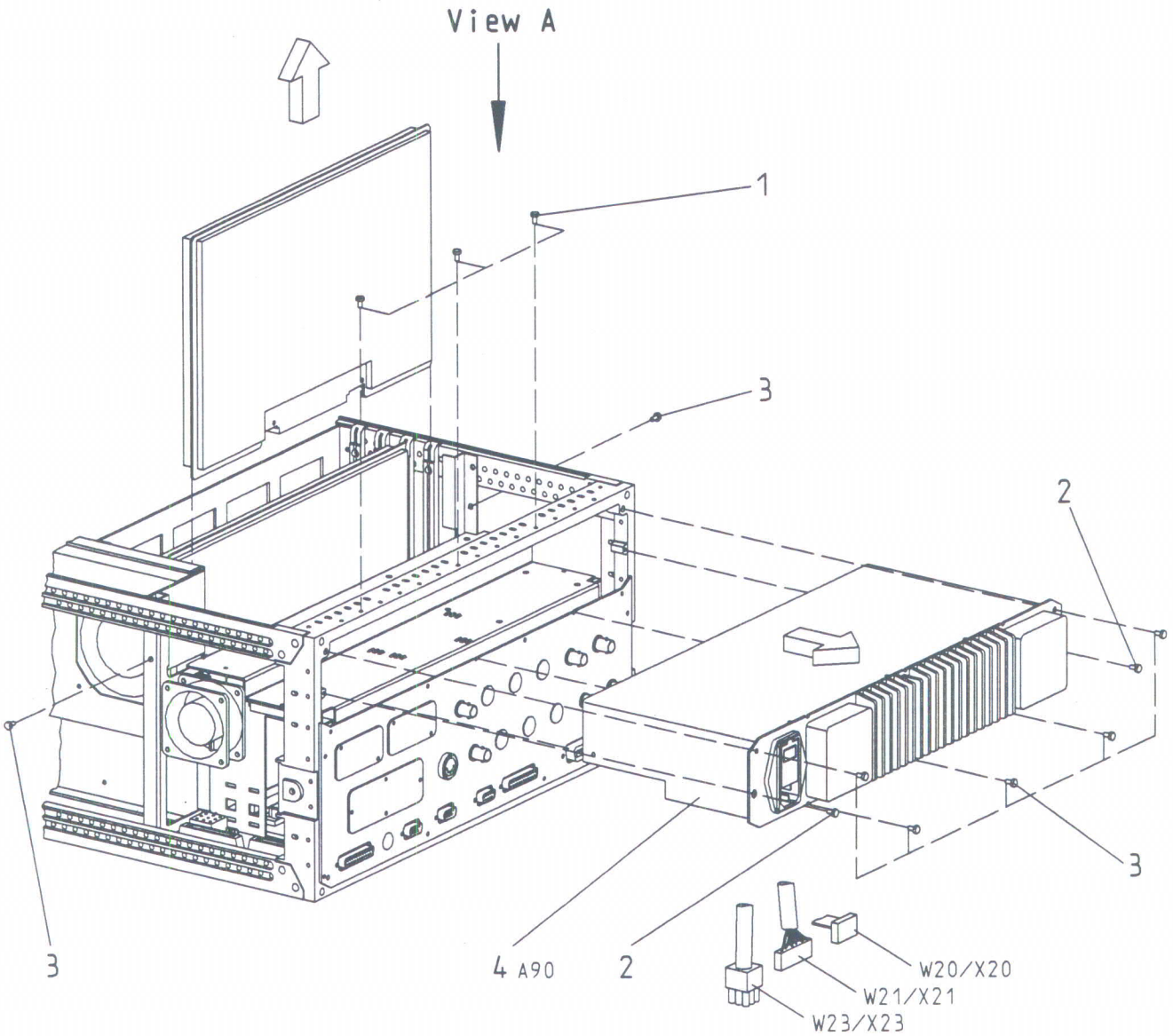
Item	Designation	Quantity	Ident. No.
1	DIN965 M3 x 8 PA	2	0396.8046.00
2	Screw with washer assembly M3 x 8	4	0071.6853.00
3	DIN7985 M3 x 12	2	0081.9090.00
4	DIN137-A3-A2	2	0005.0296.00
5	DIN9021-B3,2-A4	2	0031.5185.00
6	DIN7985 M3 x 12	4	0081.9090.00
7	DIN137-A3-A2	4	0005.0296.00
8	DIN9021-B3,2-A4	4	0031.5185.00
9	Rail	2	1065.6445.00
10	Motherboard Analog (A10)	1	1065.6516.02
11	Locking plate	2	1065.6422.00
12	Screw with washer assembly M3 x 8	4	0071.6853.00
13	Locking rail	2	1065.6416.00

6.6.4.3 Analog Moduls

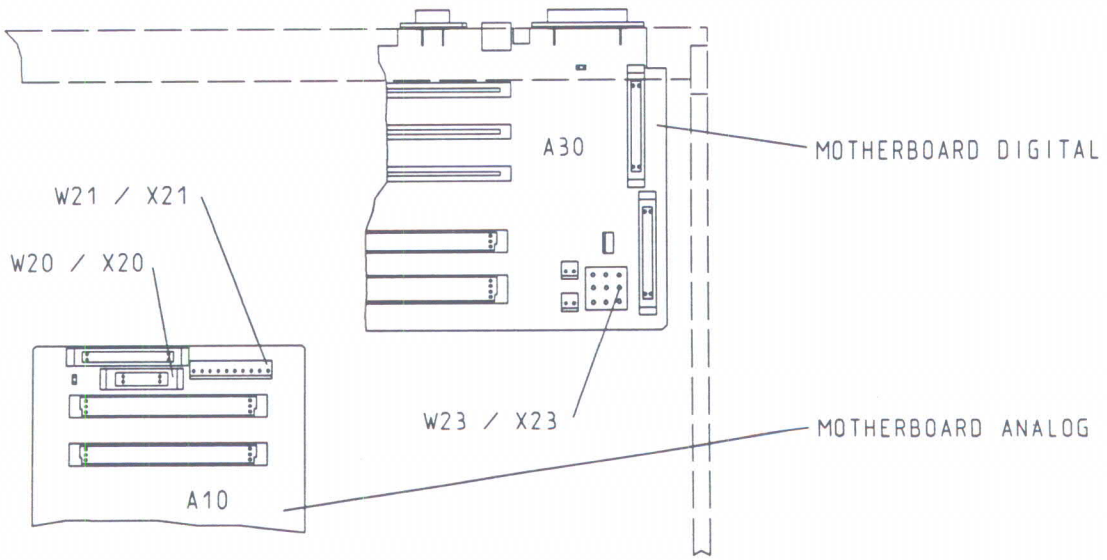




6.6.5 Power Supply Unit



View A



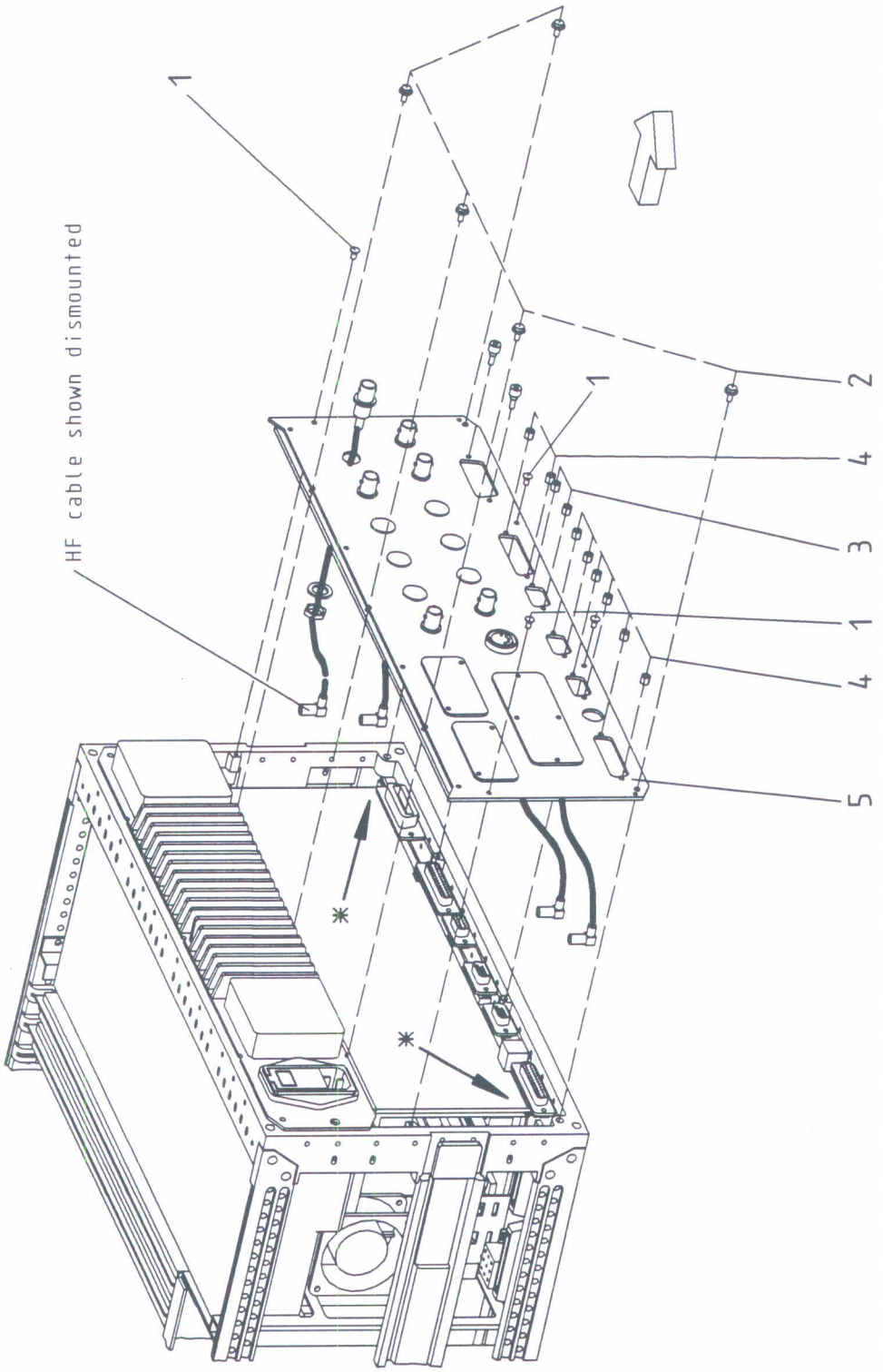
Power Supply Unit (A90)

Instructions for disassembly:
- Remove panelling according to 6.6.1
- Unlock the analog modules on A10 (see 6.6.4.1)
- Remove the last analog module (see drawing 6.6.5)
- Loosen cable W103
- Unplug cables from A10 and A30 (see drawing 6.6.5)
- Disassemble in the sequence given in the table

Caution: Do not damage cable on removing power supply unit.

Item	Designation	Quantity	Ident. No.
1	DIN965 M3 x 10 PA	3	0396.8052.00
2	DIN965 M3 x 6 PA	2	0396.8030.00
3	Screw with washer assembly M3 x 8	7	0071.6853.00
4	300-W power supply (A90)	1	1043.9941.00

6.6.6 Rear panel



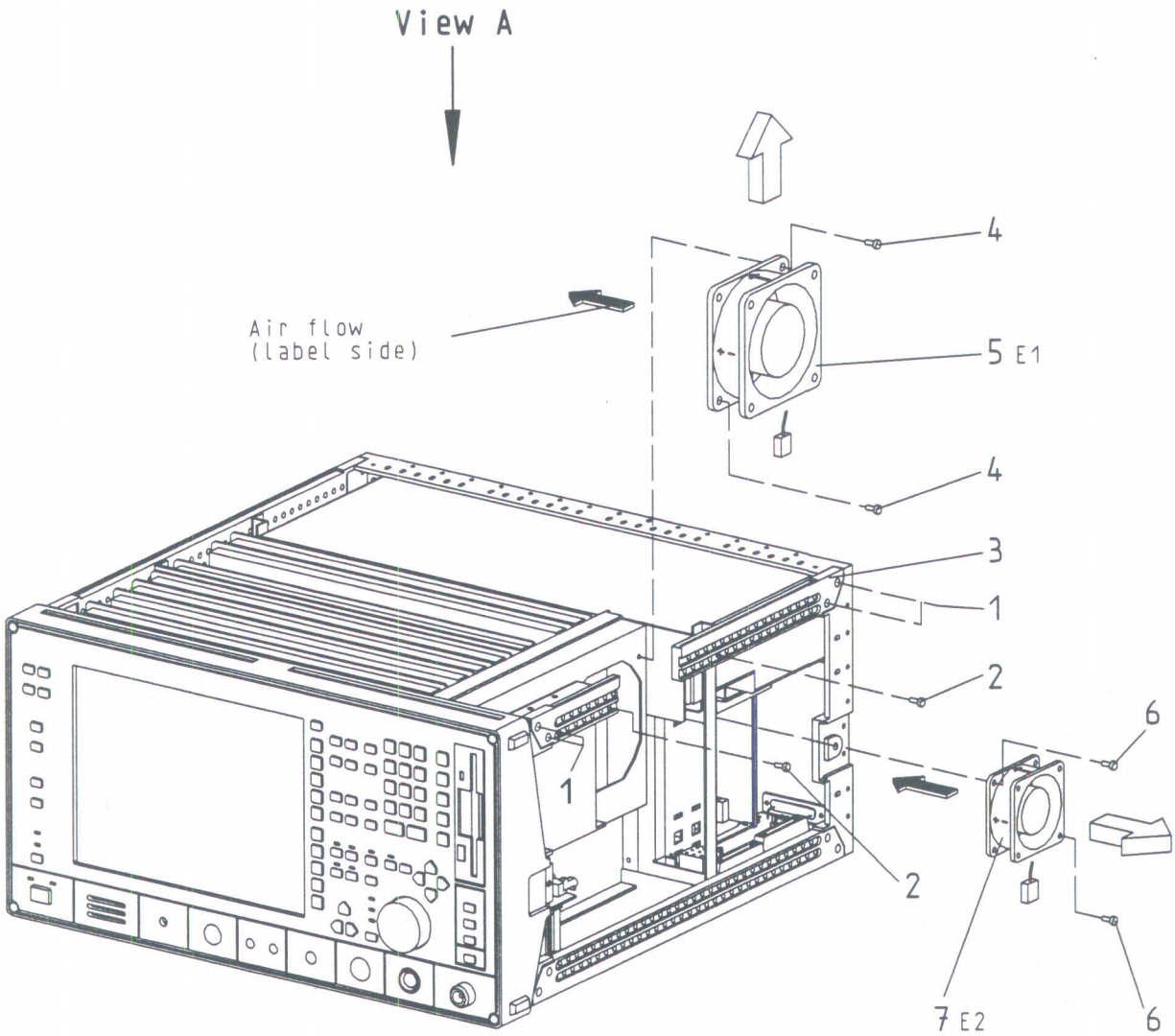
* Notch in digital motherboard to introduce RF cables

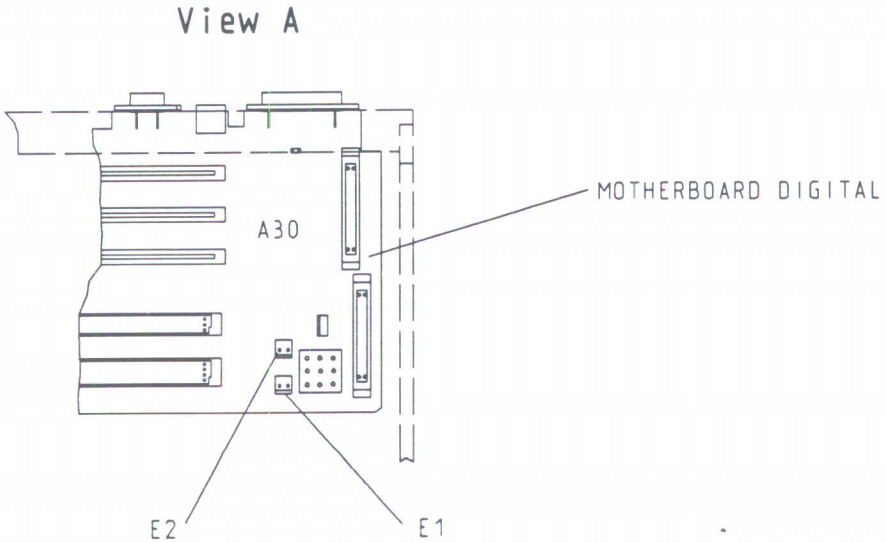
Rear Panel

Instructions for disassembly:
- Remove panelling according to 6.6.1
- Unplug cabling of analog modules
- Disassemble in the sequence given in the table

Item	Designation	Quantity	Ident. No.
1	DIN965 M3 x 6 PA	4	0396.8030.00
2	Screw with washer assembly M3 x 8	5	0071.6853.00
3	Spacer for D-Submin.	2	0243.7850.00
4	Locking bolt M3	8	0099.7783.00
5	Rear panel 1	1	1065.6468.00

6.6.7 FAN 1 (E1) / Fan 2 (E2)





Fan Disassembly (E1)

Instructions for disassembly:
- Remove panelling according to 6.6.1
- Unplug cable from motherboard A30 (see drawing 6.6.7)
- Disassemble in the sequence given in the table

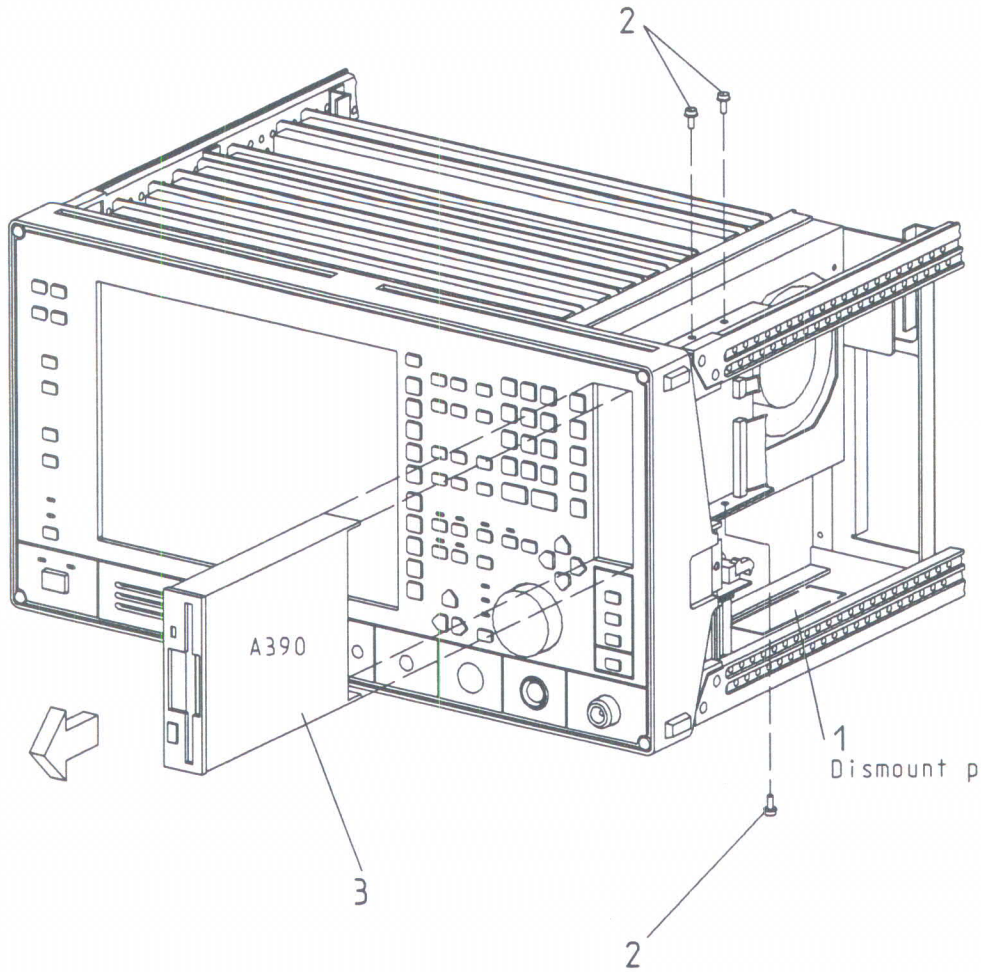
Item	Designation	Quantity	Ident. No.
1	DIN965 M3 x 8 PA	4	0396.8046.00
2	DIN7985 M3 x 10 PA	2	0396.8152.00
3	Frame rail T460	1	0396.2377.00
4	Screw with washer assembly M3 x 8	2	0071.6853.00
5	Fan 1 (E1)	1	1065.9109.00

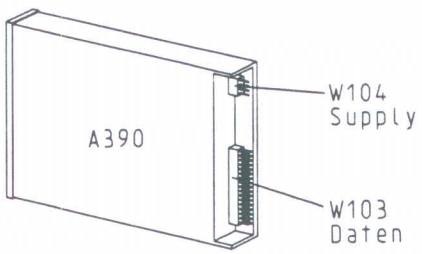
Fan Disassembly (E2)

Instructions for disassembly:
- Remove panelling according to 6.6.1
- Unplug cable from motherboard A30 (see drawing 6.6.7)
- Disassemble in the sequence given in the table

Item	Designation	Quantity	Ident. No.
6	Screw with washer assembly M3 x 8	2	0071.6853.00
7	Fan 2 (E2)	1	1065.9180.00

6.6.8 3,5"-Floppy Disk Drive (A390)





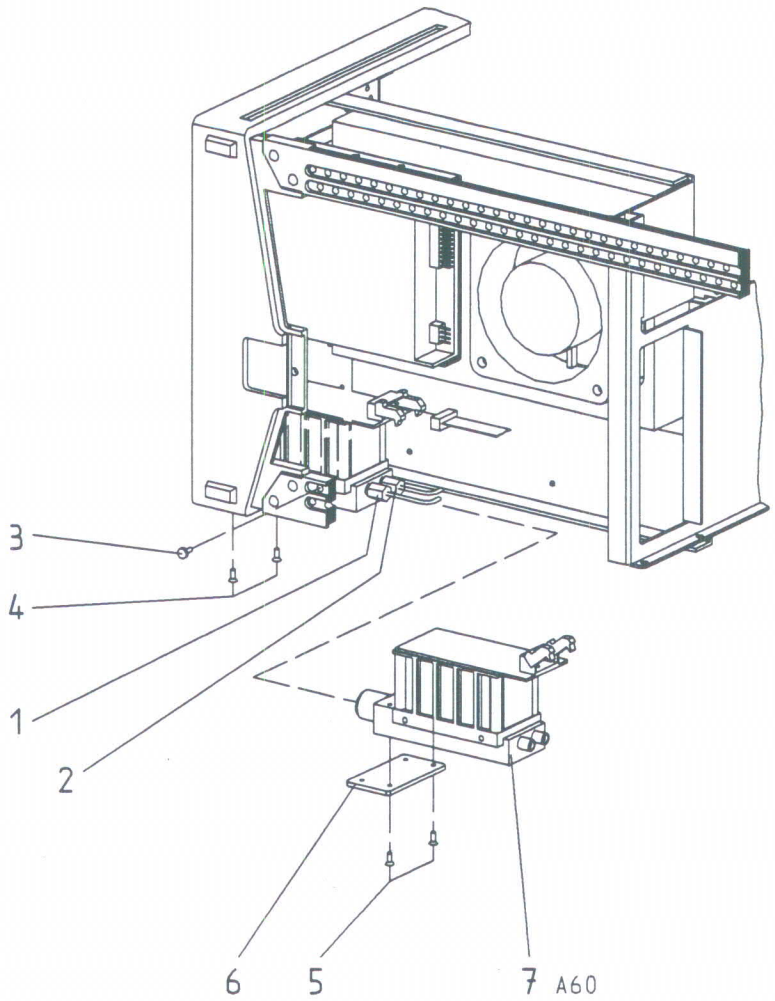
Position depending on manufacturer

3.5″ Floppy Disk Drive (A390)

Instructions for disassembly:
- Remove panelling according to 6.6.1
- Unplug cables W103 and W104 from the floppy disk drive
- Disassemble in the sequence given in the table

Item	Designation	Quantity	Ident. No.
1	Remove attenuator if necessary (see drawing)		
2	Screw with washer assembly M3 x 8	3	0071.6853.00
3	3.5″ floppy disk drive (A390)	1	0010.7308.00

6.6.9 Attenuator (A60)



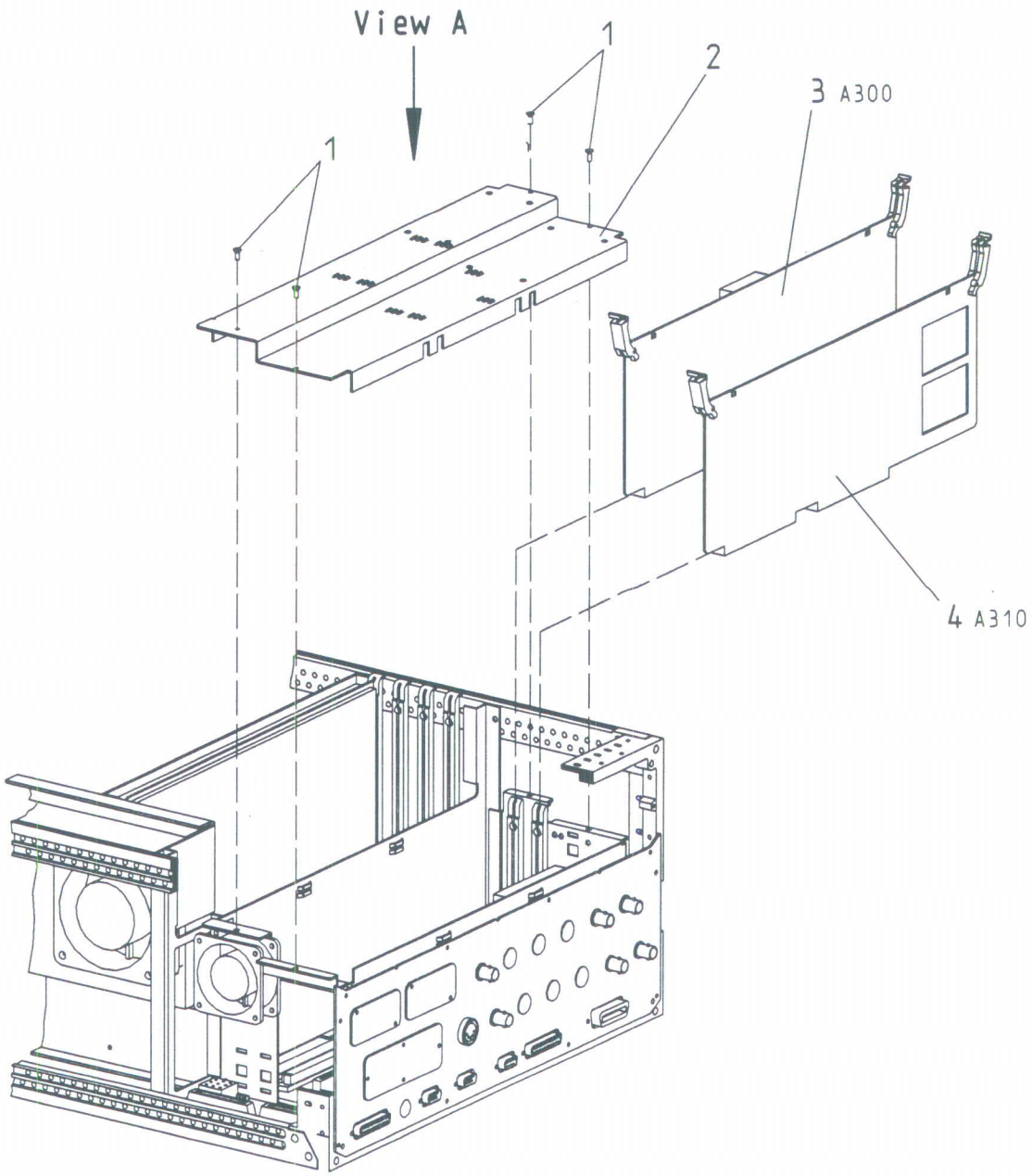
Attenuator (A60)

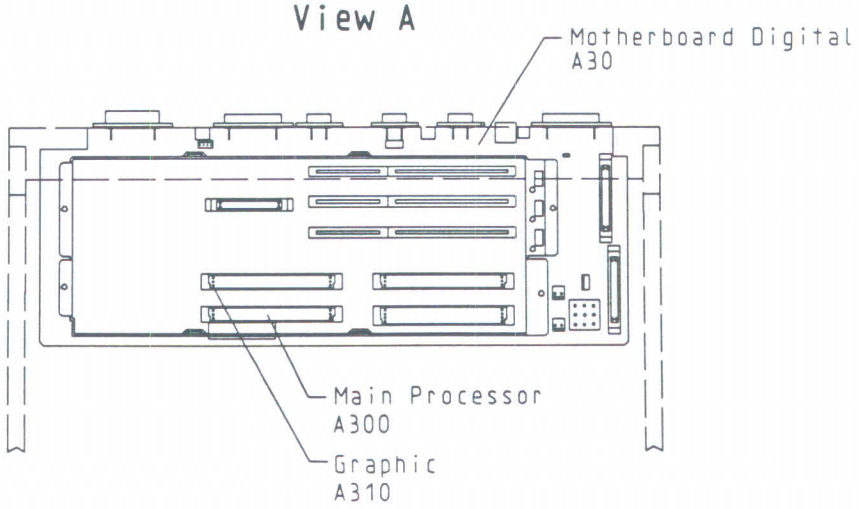
Instructions for disassembly: - Remove panelling according to 6.6.1
- Disassemble in the sequence given in the table

Item	Designation	Quantity	Ident. No.
1	RF cable W2 for FSEA 20/30	1	1065.6080.00
	RF cable W2 for FSEB 20/30	1	1066.3079.00
2	RF cable W3	1	1065.6097.00
3	DIN7985 M3 x 10 PA	1	0396.8152.00
4	DIN965 M3 x 8 PA	2	0396.8046.00
5	DIN965 M3 x 8 PA	2	0396.8046.00
6	Bearing plate	1	1065.9138.00
7	FSE attenuator (A60)	1	1067.7755.03

6.6.10 Digital Section (without own Drawing)

6.6.10.1 Shield Cover Main Processor (A300)/Graphics (A310)





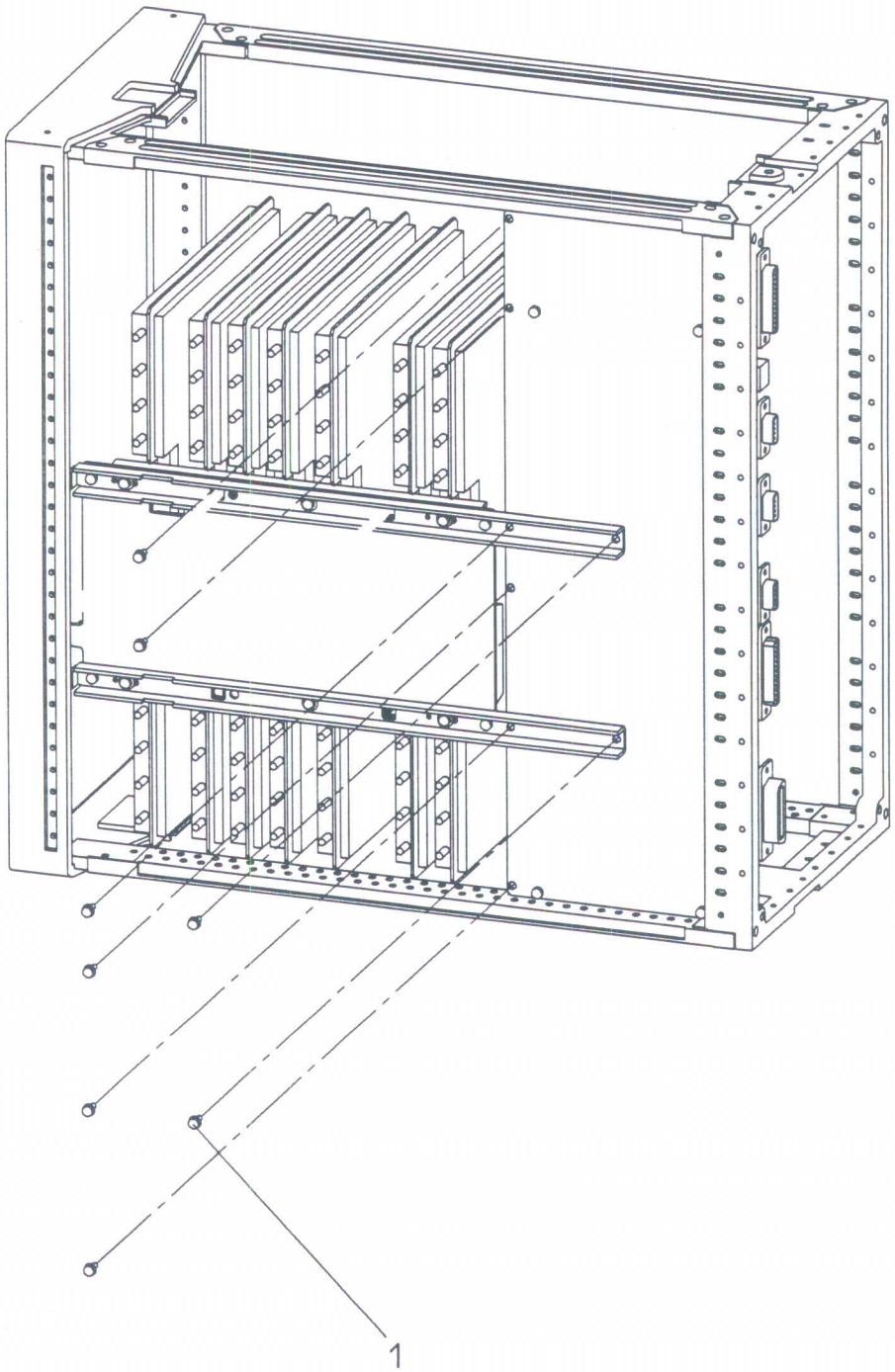
Digital Section (without own drawing)

Main Processor (A300) / Graphics (A310)

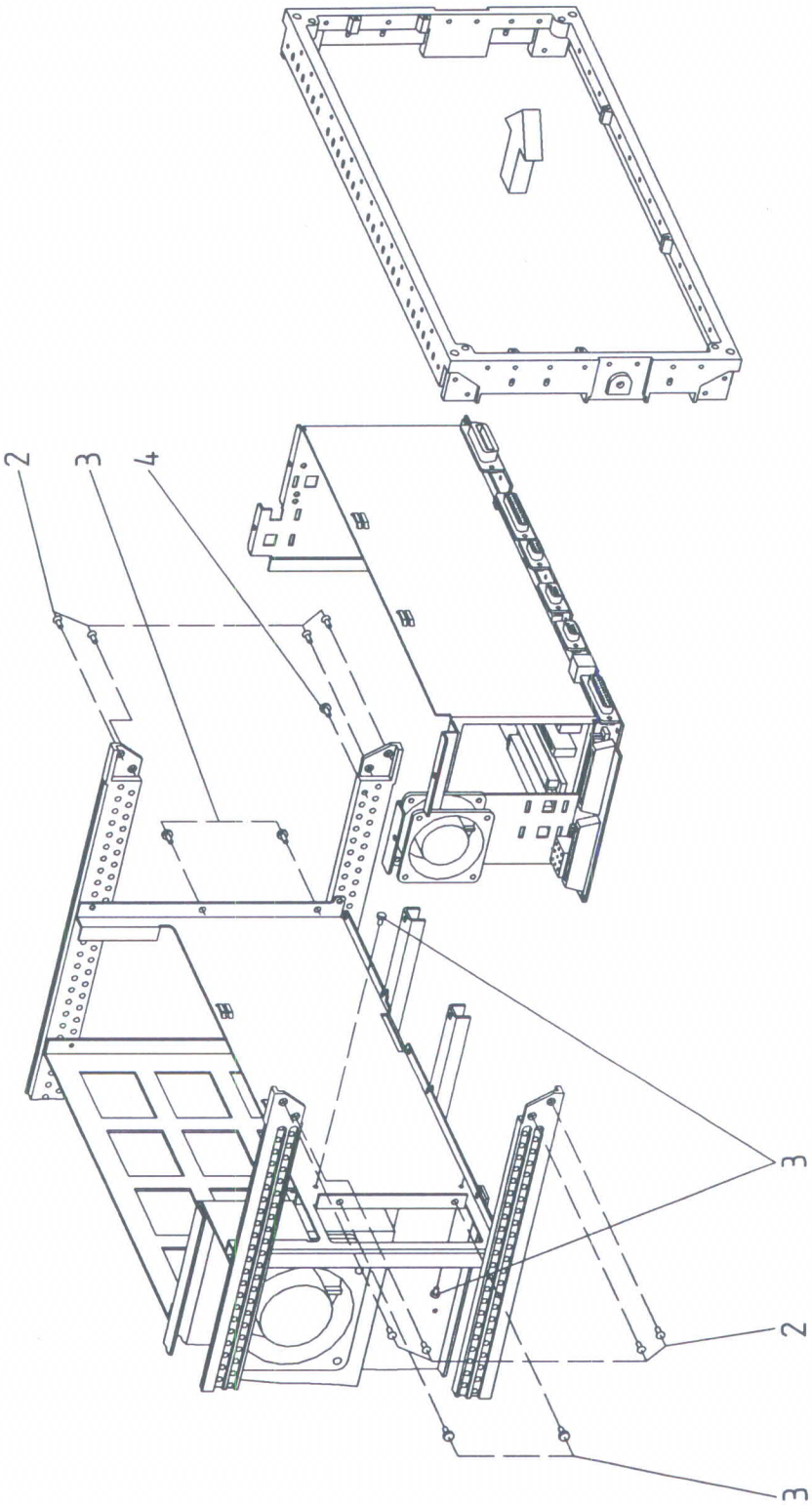
Instructions for disassembly:
- Remove panelling according to 6.6.1
- Disassemble power supply unit according to 6.6.5
- Disassemble in the sequence given in the table

Item	Designation	Quantity	Ident. No.
1	DIN965 M3 x 6 PA	4	0396.8030.00
2	Shield cover	1	1065.9067.00
3	Main Processor (A300)	1	1043.9987.03
4	Graphics (A310)	1	1043.4491.02

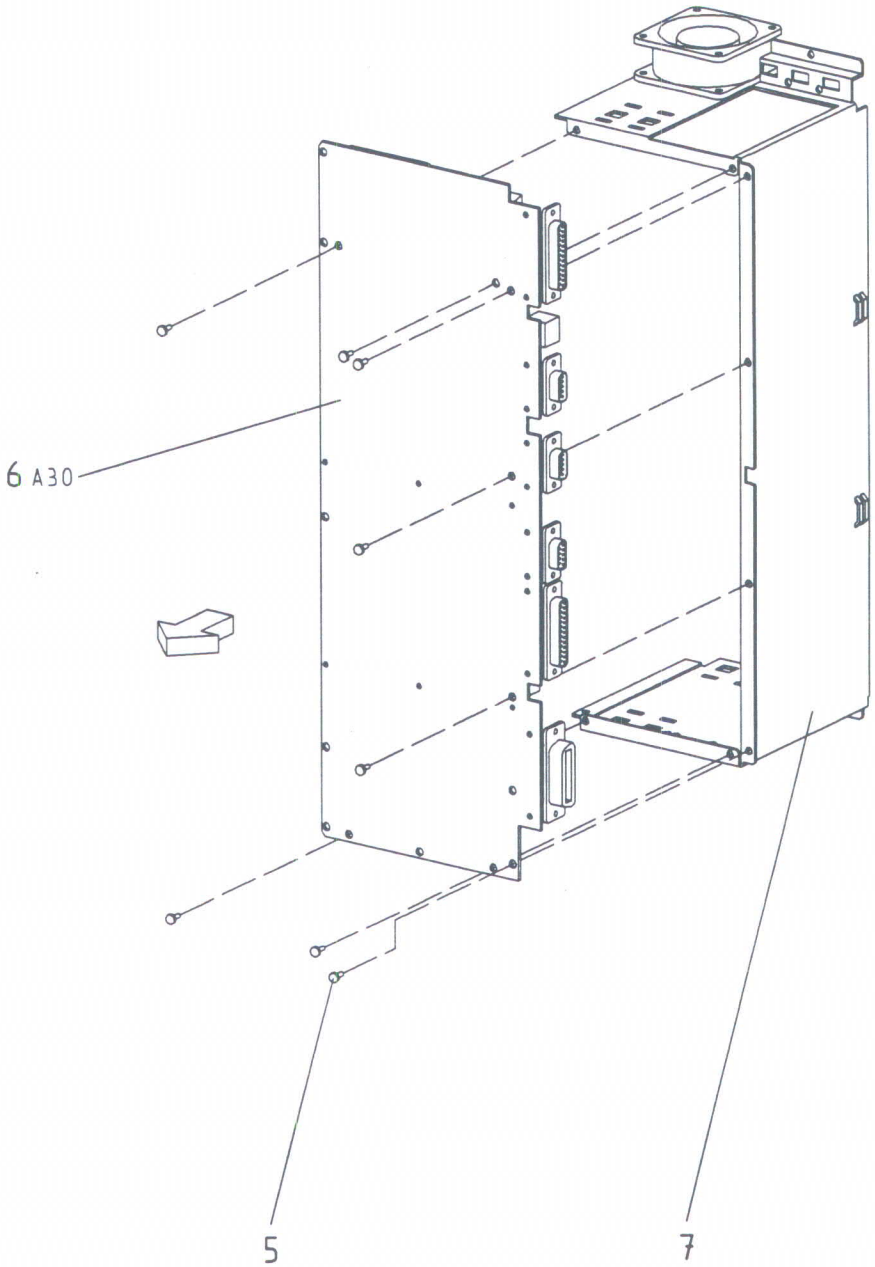
6.6.10.2 Motherboard Digital (A30)



6.6.10.2 Motherboard Digital (A30)



6.6.10.2 Motherboard Digital (A30)

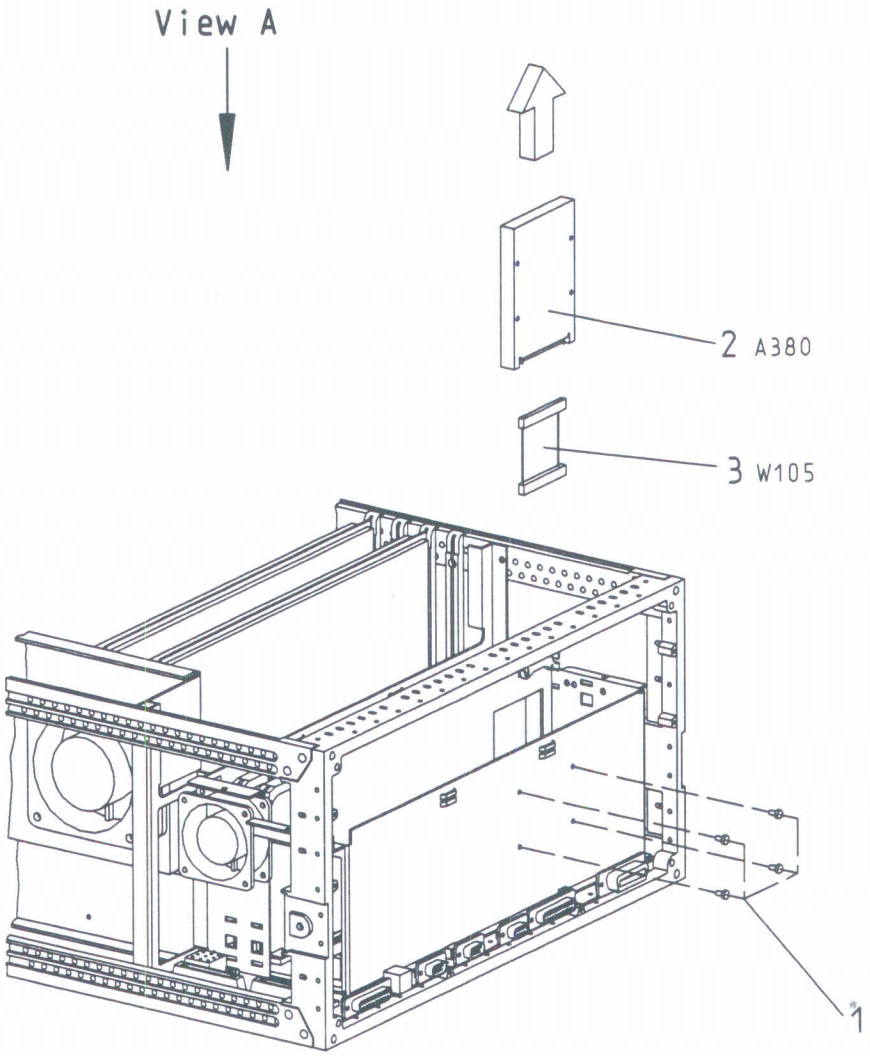


Digital Motherboard (A30)

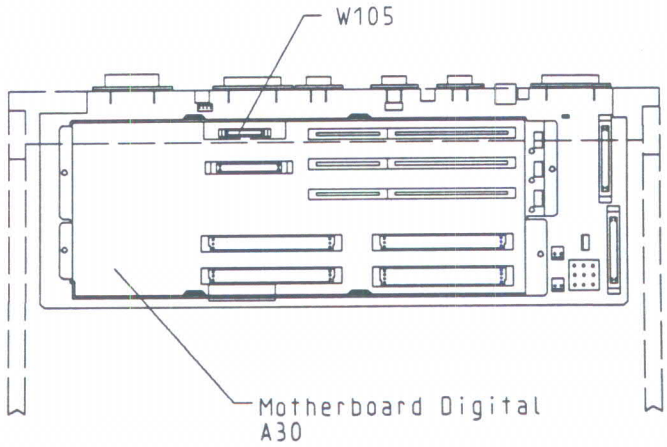
Instructions for disassembly:
- Remove panelling according to 6.6.1
- Disassemble power supply unit according to 6.6.5
- Disassemble rear plate according to 6.6.6
- Disassemble shield cover according to 6.6.10.1
- Disassemble digital modules and options according to 6.6.10
- Unplug all cables from digital motherboard
- Disassemble in the sequence given in the table

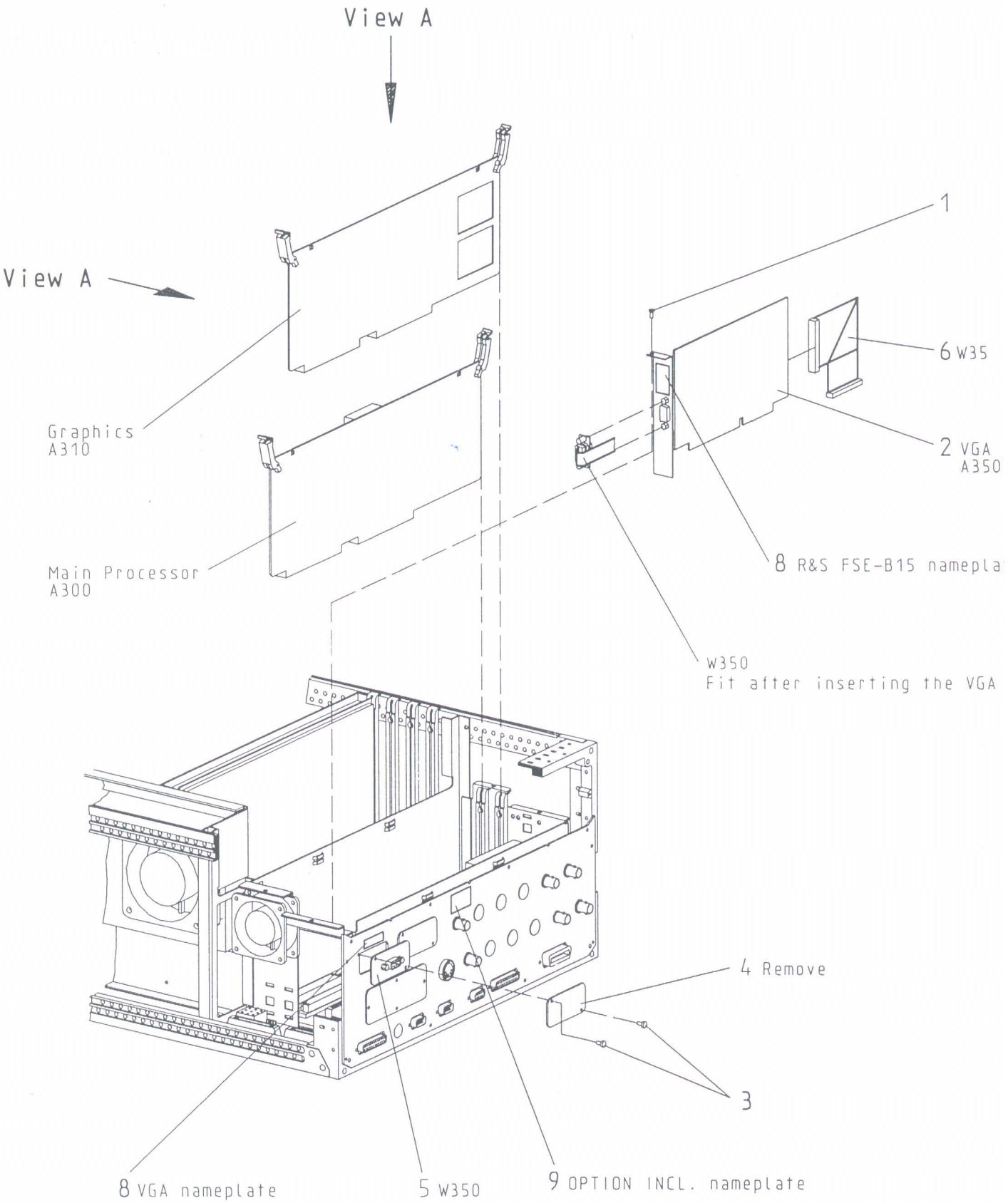
Item	Designation	Quantity	Ident. No.
1	Screw with washer assembly M3 x 8	8	0071.6853.00
2	DIN965 M3 x 8 PA	8	0396.8046.00
3	DIN7985 M3 x 6 PA	6	0396.8130.00
4	DIN7985 M3 x 10 PA	1	0396.8152.00
5	Screw with washer assembly M3 x 8	8	0071.6853.00
6	Digital motherboard (A30)	1	1065.6639.02
7	Shield casing (without fan)	1	1065.9050.00

6.6.10.3 Hard Disk (A380)



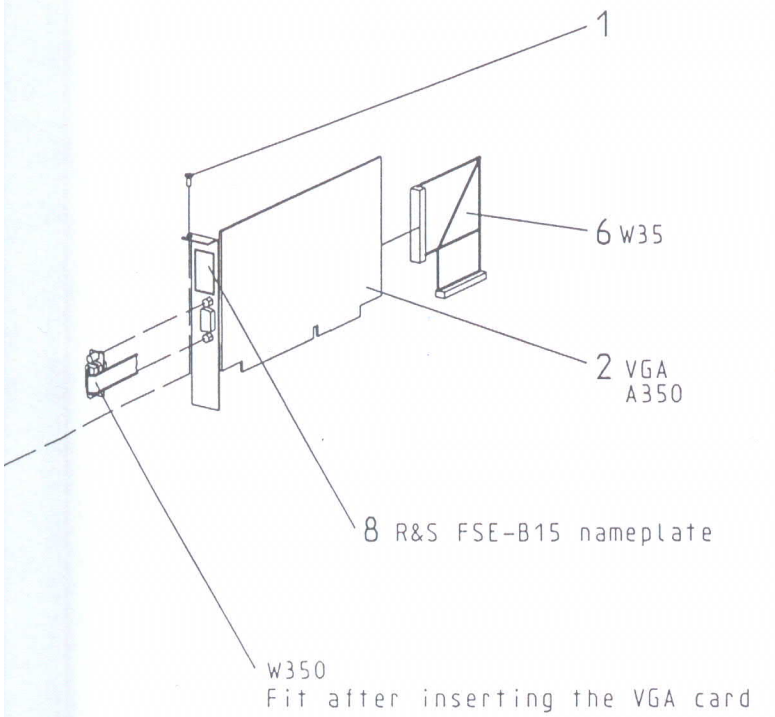
View A

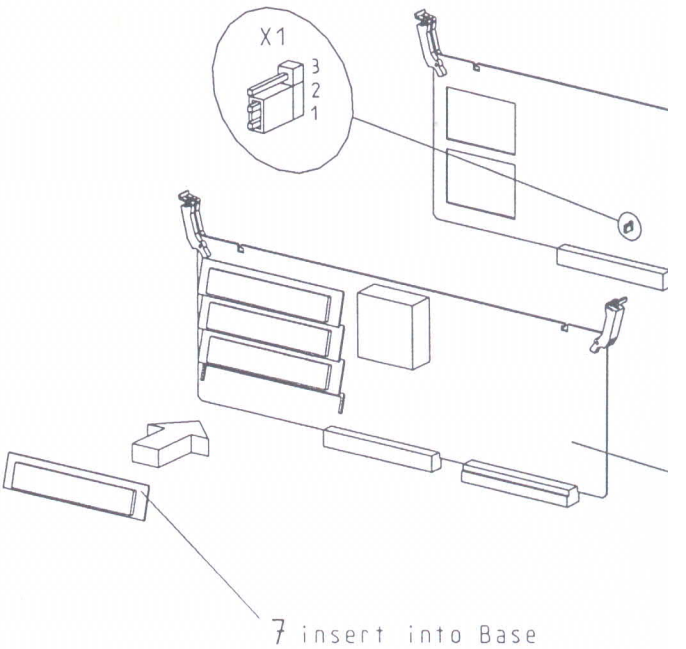


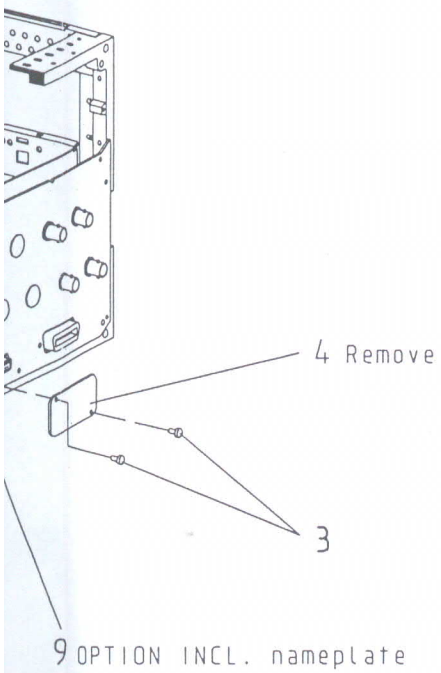

View A
View A
1
Graphics
A310
6 W35
2 VGA
A350
Main Processor
A300
8 R&S FSE-B15 nameplat
W350
Fit after inserting the VGA
4 Remove
3
8 VGA nameplate
5 W350
9 OPTION INCL. nameplate

6.6.10.4 Option FSE-B15 Co

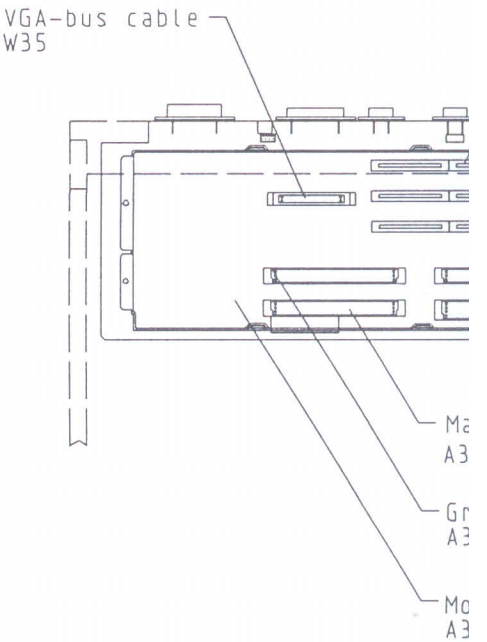
View A





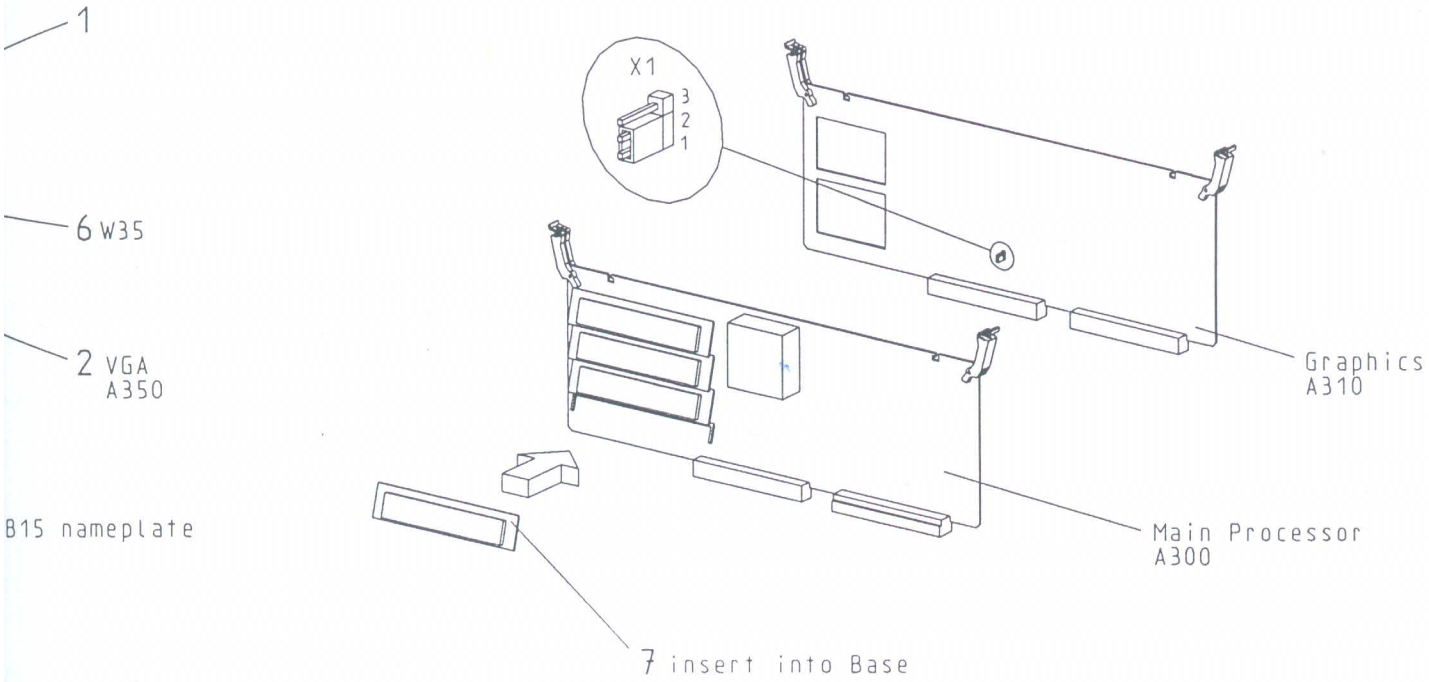


View

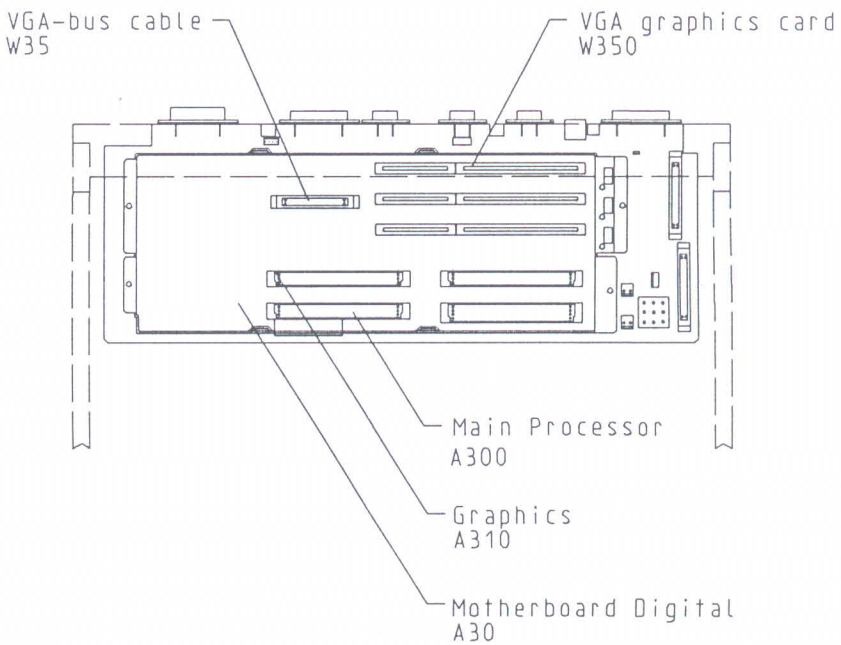


6.6.10.4 Option FSE-B15 Computer Function

View A



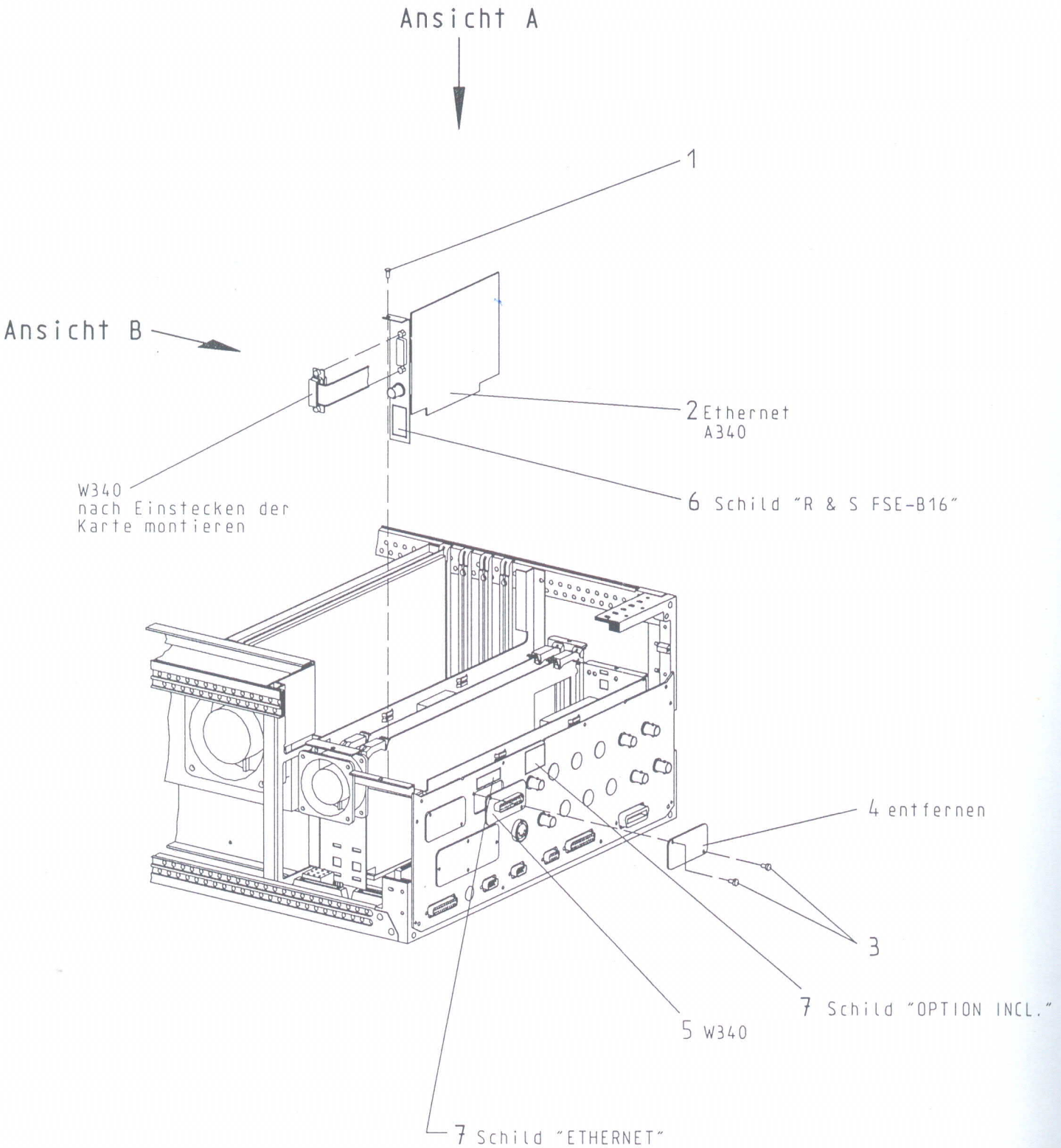
View A



4 Option FSE-B15 Computer Function

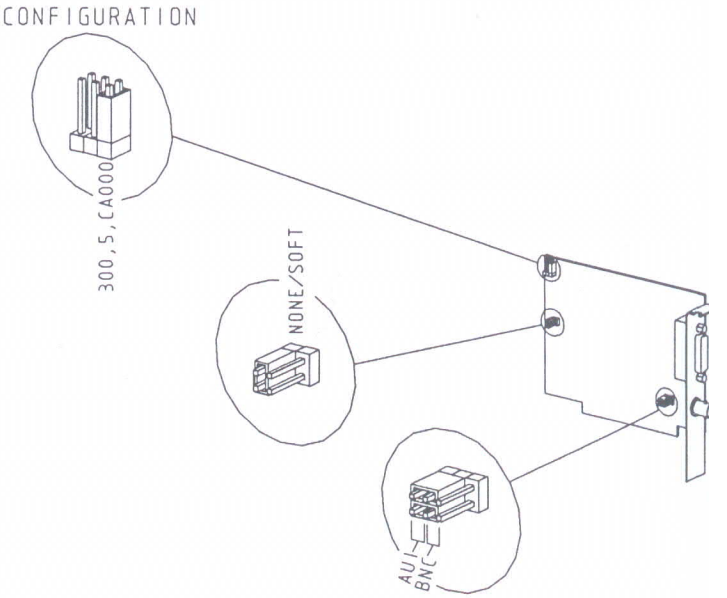
Instructions for disassembly: - Disassemble shield cover according to 6.6.10.1

Item	Designation	Quantity	Ident. No.
1	DIN84 M3 x 10 PA	1	0031.6169.00
2	VGA graphics card (A350)	1	1073.5744.02
3	Screw with washer assembly M3 x 8	2	0071.6853.00
4	Filler plate (remove)	1	1043.0550.00
5	VGA cable (W350)	1	1073.5767.00
6	VGA-bus cable (W35)	1	1043.1663.00
7	DRAM SIMM module	1	0008.8552.00
8	Set of nameplates	1	1073.5796.00
9	Option nameplate	1	1073.5773.00


Ansicht A
1
Ansicht B
2 Ethernet
A340
W340
nach Einstecken der
Karte montieren
6 Schild "R & S FSE-B16"
4 entfernen
3
7 Schild "OPTION INCL."
5 W340
7 Schild "ETHERNET"

6.6.10.5 Option FSE-B16 Etherne

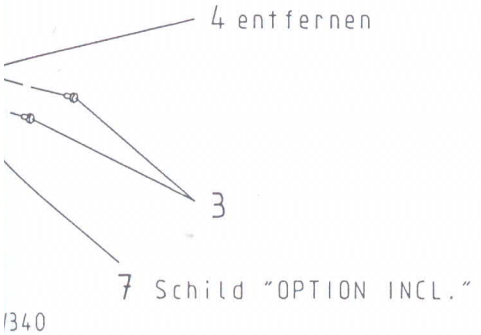
Ansicht B



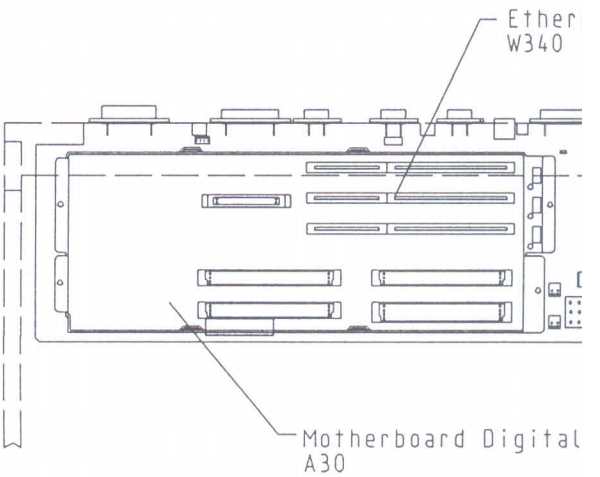
thernet
340

Schild "R & S FSE-B16"

Ansicht A

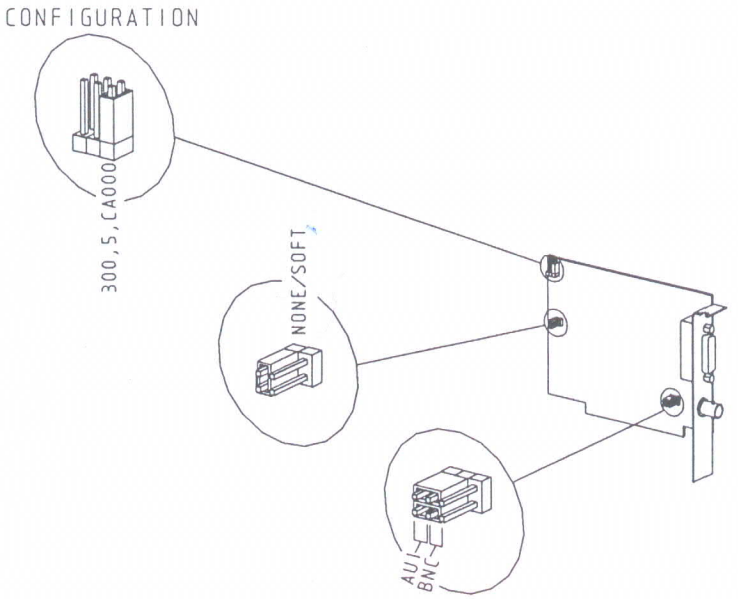


/340

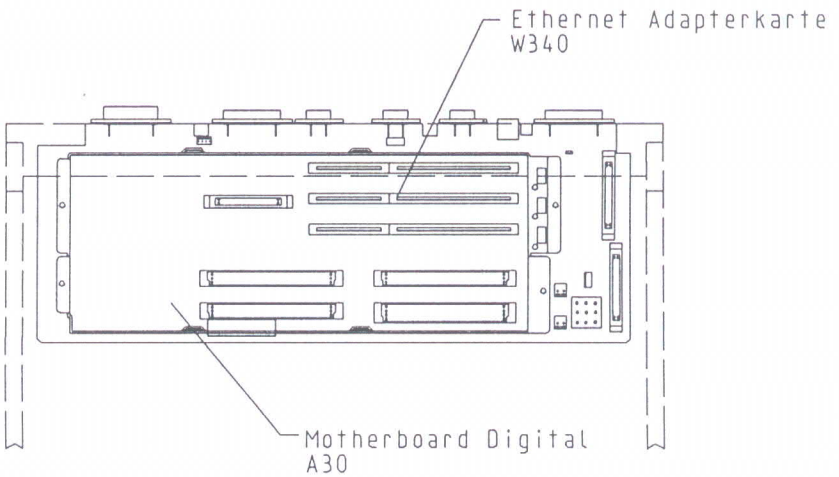


6.6.10.5 Option FSE-B16 Ethernet VAR02

Ansicht B



Ansicht A

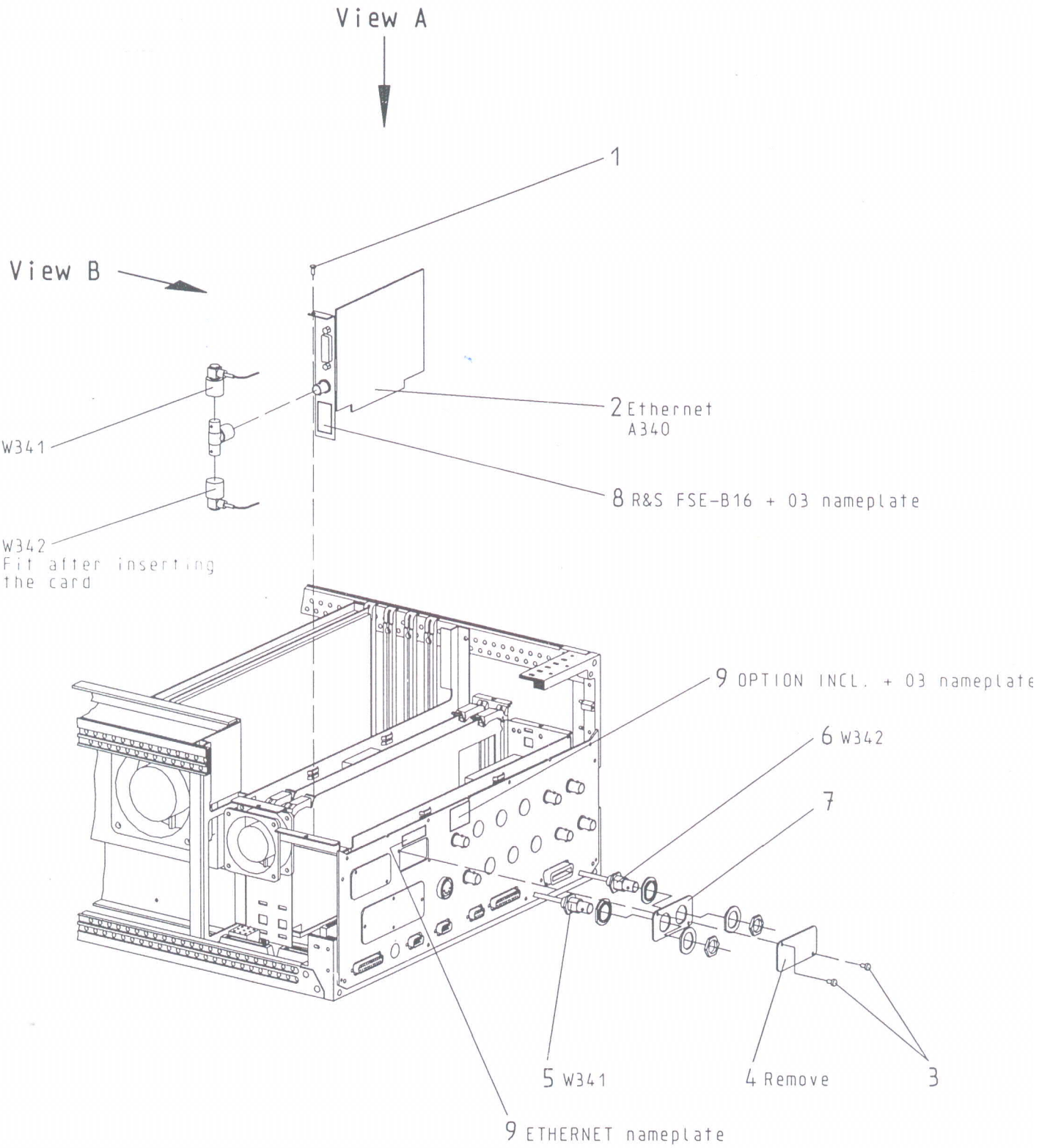


INCL."

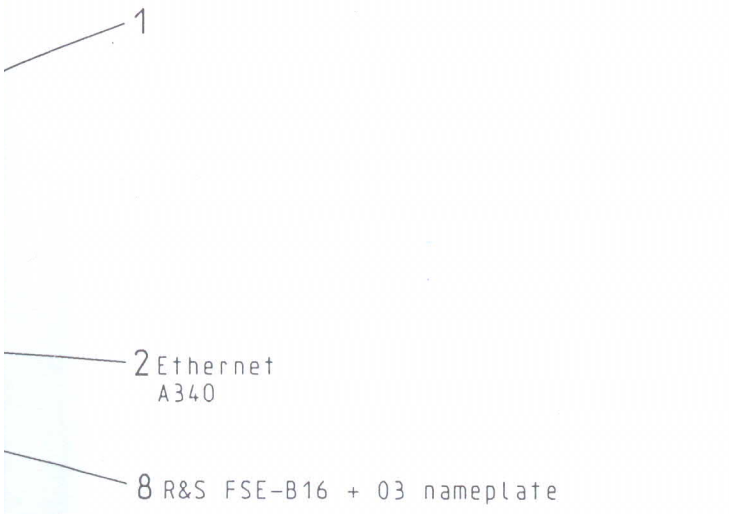
Option FSE-B16 Ethernet VAR02

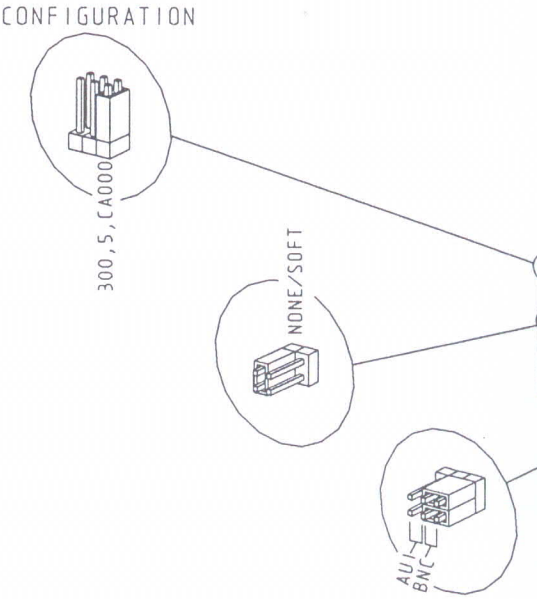
Instructions for disassembly: - Disassemble shield cover according to 6.6.10.1

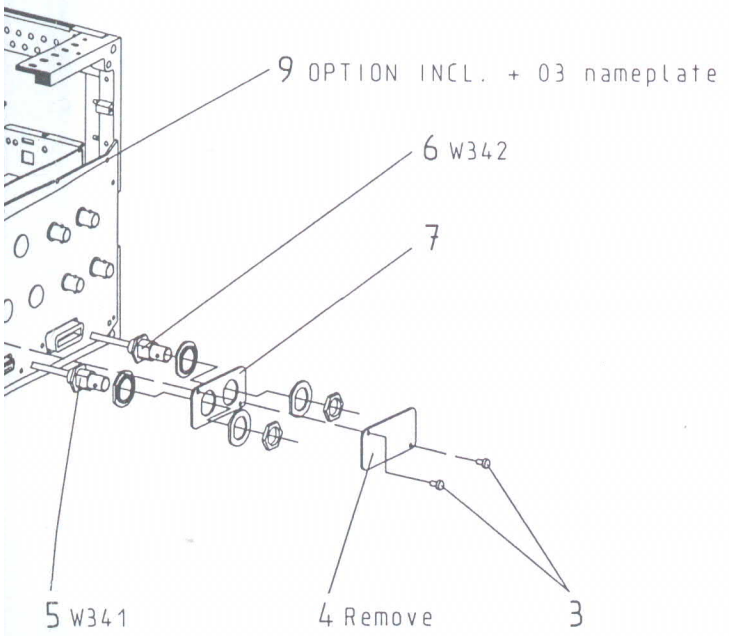
Item	Designation	Quantity	Ident. No.
1	DIN84 M3 x 10 PA	1	0031.6169.00
2	Ethernet adapter card (A340)	1	1028.9050.00
3	Screw with washer assembly M3 x 8	2	0071.6853.00
4	Filler plate (remove)	1	1043.0550.00
5	LAN-SUBD 15 cable (W340)	1	1043.1705.00
6	Set of nameplates	1	1073.5909.00
7	Option nameplate	1	1073.5896.00


View A
1
View B
2 Ethernet
A340
W341
8 R&S FSE-B16 + 03 nameplate
W342
Fit after inserting
the card
9 OPTION INCL. + 03 nameplate
6 W342
7
5 W341
4 Remove
3
9 ETHERNET nameplate

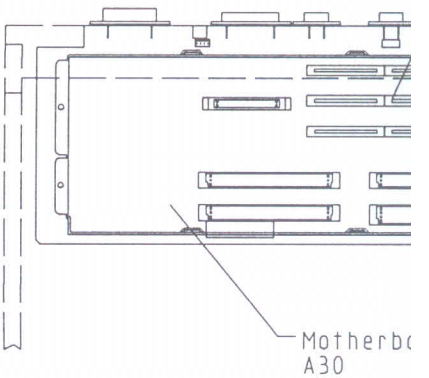
View


1
2 Ethernet
A340
8 R&S FSE-B16 + 03 nameplate


CONFIGURATION
300,5,CA000
NONE/SOFT
AUI
BNC

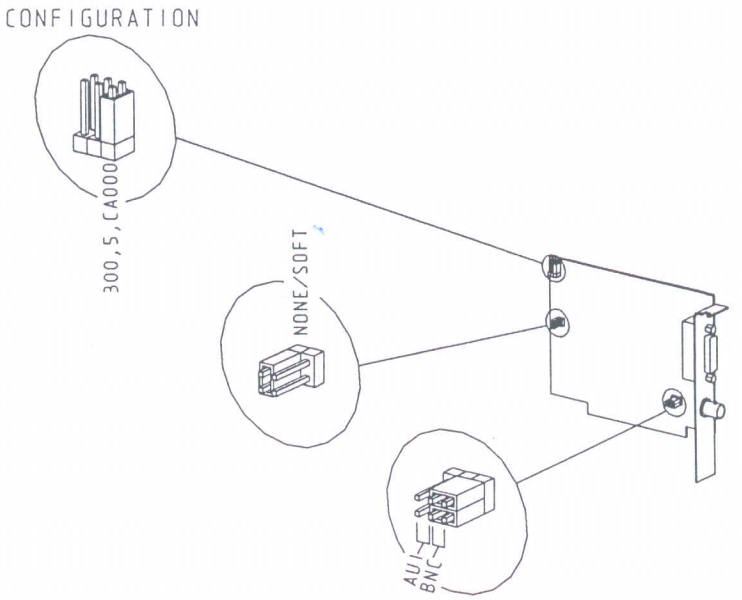

9 OPTION INCL. + 03 nameplate
6 W342
7
5 W341
4 Remove
3
9 ETHERNET nameplate

View A


Motherbo
A30

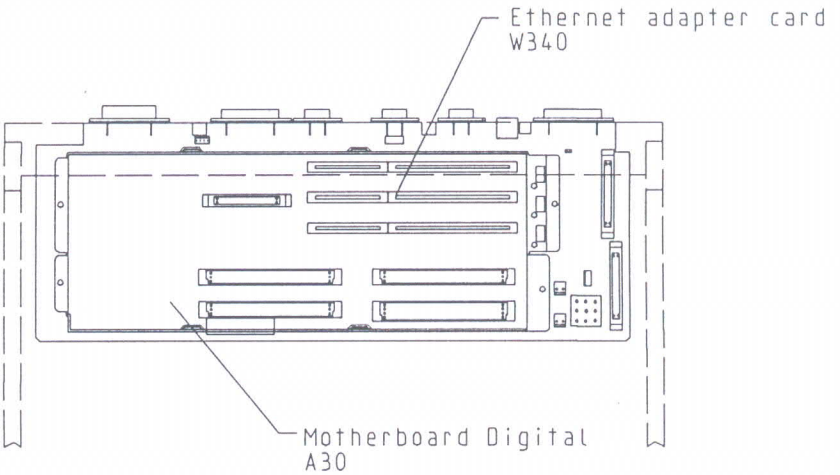
6.6.10.6 Option FSE-B16 Ethernet VAR03

View B



)3 nameplate

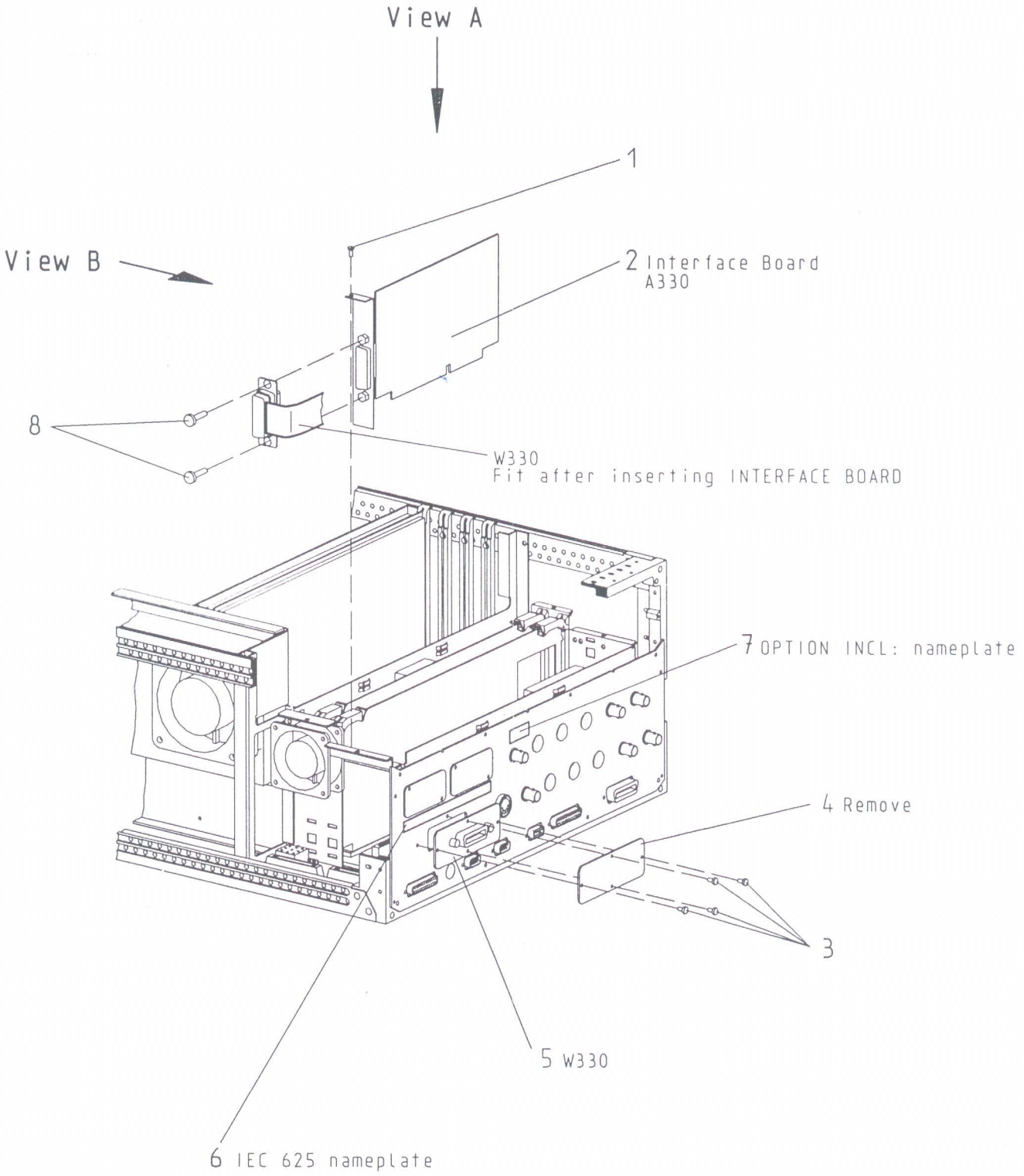
View A



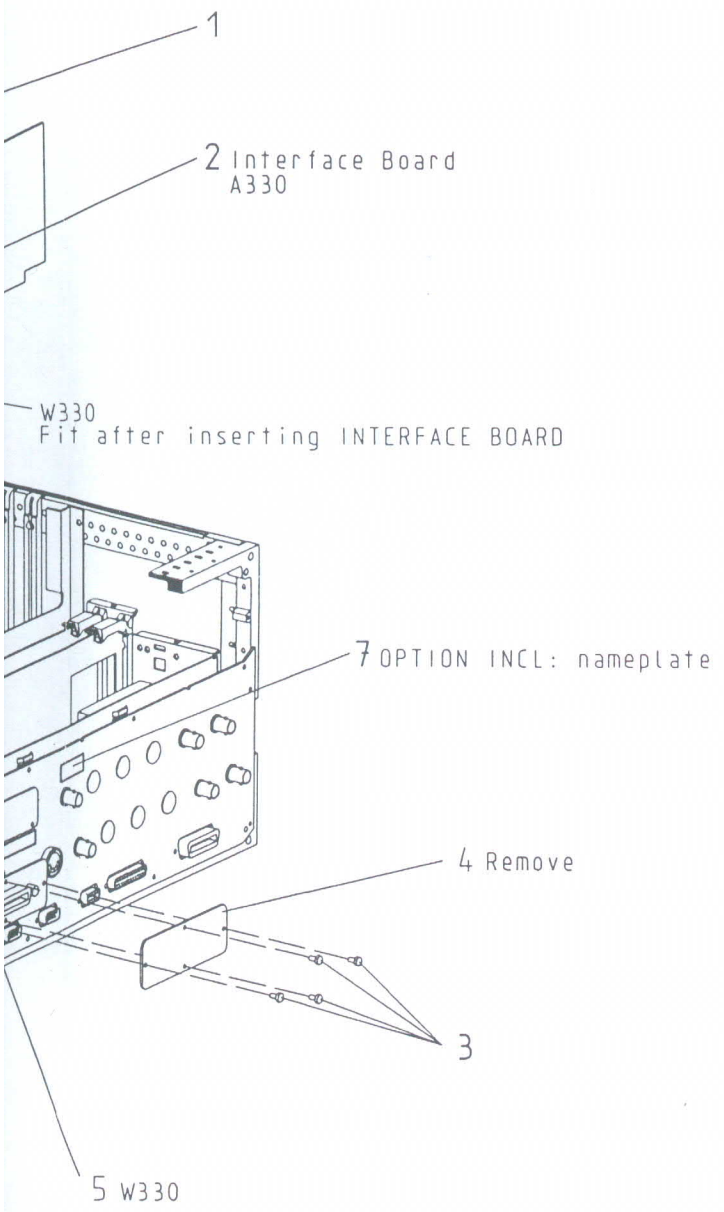
Option FSE-B16 Ethernet VAR03

Instructions for disassembly: - Disassemble shield cover according to 6.6.10.1

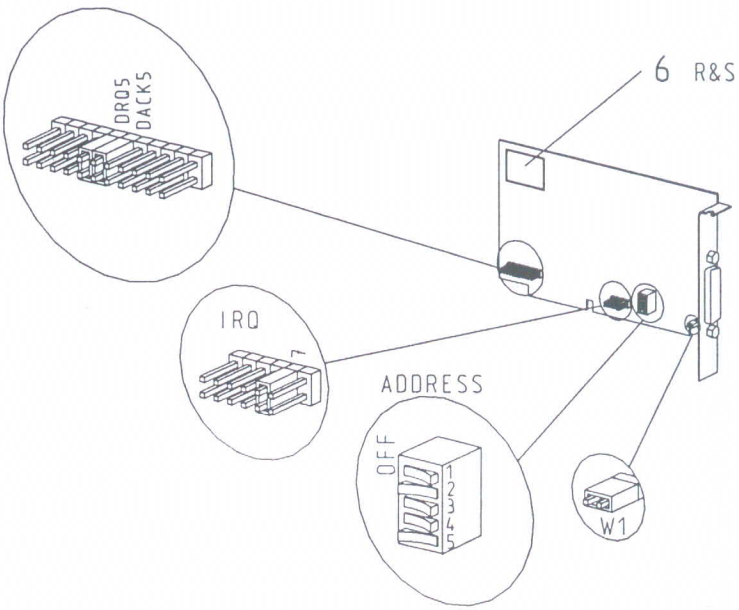
Item	Designation	Quantity	Ident. No.
1	DIN84 M3 x 10 PA	1	0031.6169.00
2	Ethernet adapter card (A340)	1	1028.9050.00
3	Screw with washer assembly M3 x 8	2	0071.6853.00
4	Filler plate (remove)	1	1043.0550.00
5	LAN cable (W341)	1	1043.1711.00
6	LAN cable (W342)	1	1043.1728.00
7	BNC plate	1	1043.0573.00
8	Set of nameplates	1	1073.5909.00
9	Option nameplate	1	1073.5896.00


View A
1
View B
2 Interface Board
A330
8
W330
Fit after inserting INTERFACE BOARD
7 OPTION INCL: nameplate
4 Remove
3
5 W330
6 IEC 625 nameplate

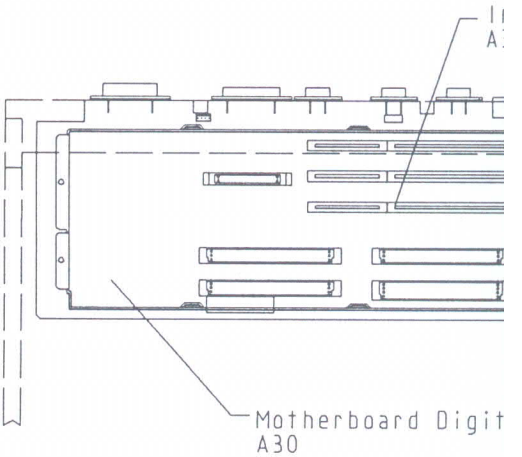
A



View B

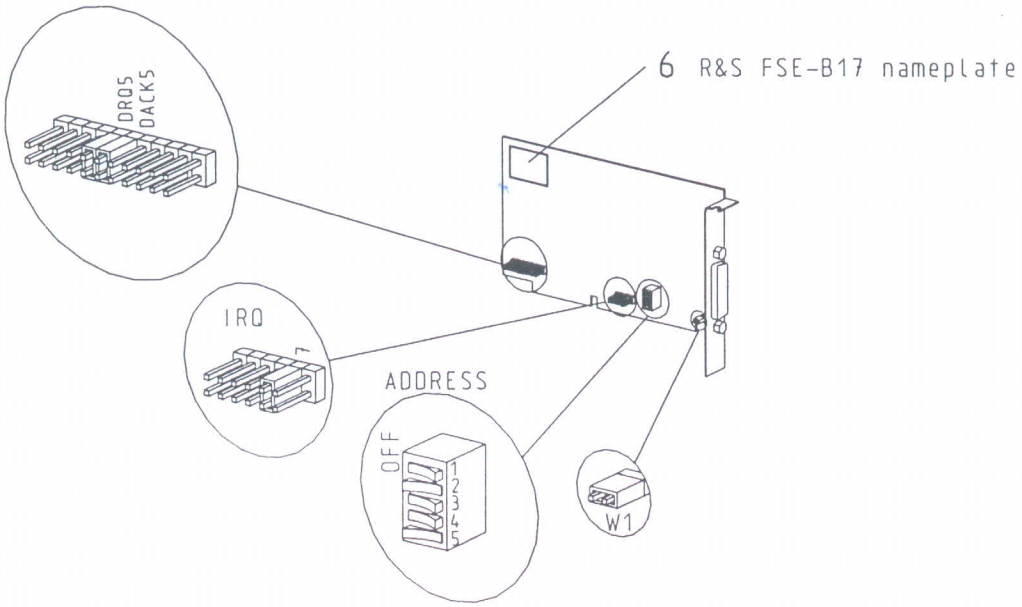


View A



6.6.10.7 Option FSE-B17
IEC-BUC for Computer Funktion

View B

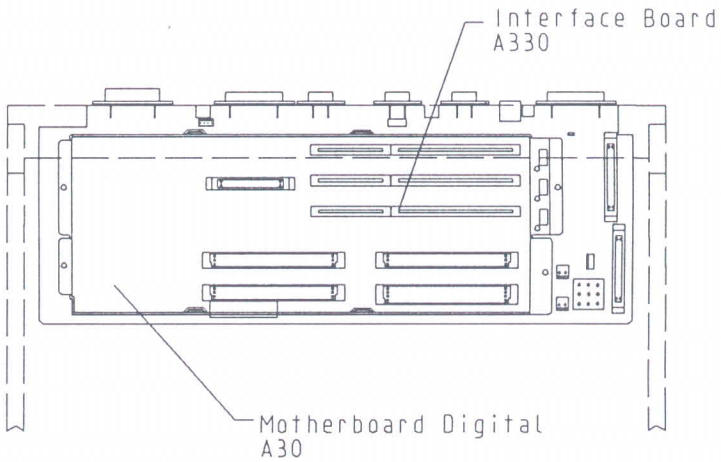


RD

L: nameplate

ove

View A



Option FSE-B17 IEC Bus

Instructions for disassembly: - Disassemble shield cover according to 6.6.10.1

Item	Designation	Quantity	Ident. No.
1	DIN84 M3 x 10 PA	1	0031.6169.00
2	AT-GPIB interface board (A330)	1	1064.1440.00
3	Screw with washer assembly M3 x 8	4	0071.6853.00
4	Filler plate (remove)	1	1065.9096.00
5	IEC-bus cable (W330)	1	1066.4023.00
6	Set of nameplates	1	1066.4052.00
7	Option nameplate	1	1066.4069.00
8	DIN84 M3.5 x 10	2	0005.1205.00

ROHDE&SCHWARZ

Schlüsselliste
für Bauteile-Sachnummern
Code list
for component stock Nos.
Liste
des références des composants

(R 29500 Bl 5)
095.1000 Bl. 5

ROHDE&SCHWARZ

R&S-Schlüsselliste
R&S key list
Liste des symboles de référence R&S

Die R&S-Schaltteillisten nennen in der Spalte "Benennung/Beschreibung" die technischen Daten der Bauelemente in Kurzform. Die Art des Bauelements (z.B. Schicht-, Draht-Widerstand usw.) beschreiben die 2 Kennbuchstaben vor der "Benennung" (evtl. auch vor der "Sachnummer"), die nachfolgend erklärt werden. In Ersatzteil-Bestellungen an R&S ist stets die Angabe der vollständigen Sachnummer erforderlich.

The R&S Parts Lists give the technical data of the components in short form in the column "Benennung/Beschreibung" (designation). The type of component (e.g. depos.-carbon resistor, wire-wound resistor etc.) is indicated by 2 identification letters before the designation, possibly also before the "Sachnummer" (order number), which are explained below. When ordering spare parts from R&S, the complete order number must always be specified.

La colonne «Désignation/description» des listes de pièces de R&S indique les caractéristiques des éléments sous forme abrégée. Le type d'élément (p.ex. résistance à couche, résistance bobinée etc. ...) est décrit par les deux lettres précédant la désignation (et éventuellement le numéro de référence), dont voici l'explication. Prière d'indiquer le numéro de référence («Sachnummer») complet dans toute commande de pièces de rechange.

Teile-familie	Art des Bauelementes	Parts family	Type of component	Famil-le	Type d'element
A	**Aktive Bauelemente, Halbleiter**	**A**	**Active components, semiconductors**	**A**	**Composants actifs, semiconducteurs**
AD	Universaldiode, z.B. Gleichrichter, Sperrdiode	AD	General-purpose diode, e.g. rectifier, high-resistance diode	AD	Diode d'usage général, p.ex. redresseur, diode à haute résistance
AE	Spezialdiode, z.B. Tunnel-, Kapazitäts-, Zener-Diode	AE	Diode (special), e.g. tunnel diode, varactor, Zener diode	AE	Diode spéciale, p.ex. diode tunnel, varactor, diode Zener
AF	Fotohalbleiter, z.B. Foto-Diode, -Transistor, -Widerstand, Leuchtdiode	AF	Photo-semiconductor, e.g. resistor, diode, transistor, LED	AF	Semiconducteur photoélectrique, p.ex. diode, transistor, résistance photoél., DEL
AG	Leistungs-Gleichrichter, z.B. Thyristor, Triac, Selengleichrichter	AG	Power rectifier, e.g. thyristor, triac, selenium rectifier	AG	Redresseur de puissance, p.ex. thyristor, triac, redresseur, au sélénium
AK	Kleinsignal-Transistor	AK	Small-signal transistor	AK	Transistor faible puissance
AL	Leistungs-Transistor	AL	High-power transistor	AL	Transistor grande puissance
AM	Spezial-Transistor, z.B. FET, MOSFET	AM	Transistor (special), e.g. FET, MOS-FET	AM	Transistor spécial, p.ex. TEC, MOSTEC
AP	Peltier-, Hall-Element	AP	Peltier element, Hall element	AP	Element Peltier, élement Hall
AR	Rohre für Empfänger, Verstärker, Gleichrichter	AR	Valve for receiver, amplifier, rectifier	AR	Tube pour récepteur, amplificateur, redresseur
AS	Spezialrohre, z.B. Senderöhre, EW-Widerstand, Stabilisator	AS	Valve (special), e.g. for transmitter, baretter, ballast valve	AS	Tube (spécial), p.ex. pour émetteur, résistance fer-hydrogène, ballast
AT	Katodenstrahlrohre, z.B. Bildröhre, Ziffern-Anzeigeröhre	AT	Cathode ray tube, e.g. picture tube, digital indicator tube	AT	Tube à rayon cathodique, p.ex. tube à image, tube à affichage numérique
AZ	Zubehör für Halbleiter u. Rohren	AZ	Accessories for semiconductors and valves	AZ	Accessoires pour semiconducteurs et tubes
B	**Bausteine**	**B**	**PC boards, chips**	**B**	**Cartes imprimées, puces**
BC	Integr. Schaltkreis (Microcomp.)	BC	Integrated circuit (interface, A/D)	BC	Circuit intégré (microprocesseur)
BD	R&S-Dünnschicht- und Dickschichtschaltung	BD	R&S thinfilm or thickfilm circuit	BD	Circuit R&S à couche mince ou épaisse
BG	R&S-spezifische Gate-Arrays	BG	R&S gate arrays	BG	Circuits intégrés prédiffusés R&S
BJ	Integrierter Schaltkreis (Interface, A/D-Wandler)	BJ	Integrated circuit (interface, A/D converter)	BJ	Circuit intégré (interface, convertisseur A/N)
BL	Log. Schaltkreis z.B. DTL, TTL, HTL, ECL, C-MOS	BL	Logic circuit, e.g. DTL, TTL, HTL, ECL, C-MOS	BL	Circuit logique, p.ex. DTL, TTL, HTL, ECL, C-MOS
BM	Hybridbaustein, z.B. Mischer, Tuner, Modulator	BM	Hybrid chip, e.g. mixer, tuner, modulator	BM	Puce hybride, p.ex. mélangeur, tuner, modulateur
BO	Analogschaltkreis, z.B. Operationsverstärker	BO	Analog circuit, e.g. operational amplifier	BO	Circuit analogique, p.ex. amplificateur opérationnel
BP	Optoelektronischer Baustein, z.B. Anzeigeeinheit, Koppler	BP	Optoelectronic component, e.g. display, coupler	BP	Composant optoélectronique, p.ex. afficheur, coupleur
BS	Schalt- und Steuerbaustein, elektronischer Sensor	BS	Switching and control modul, electronic sensor	BS	Modul de commutation et de commande, sonde électronique
BV	Stromversorgung, Übersp.-Schutz	BV	Power pack, protective circuit	BV	Alimentation, protection surcharge
BZ	Zubehör	BZ	Accessories	BZ	Accessoires

R&S-Schlüsselliste
R&S key list
Liste des symboles de référence R&S

ROHDE&SCHWARZ

Teile-familie	Art des Bauelementes	Parts family	Type of component	Famille	Type d'element
F	**Fassungen, Steckverbindungen**	**F**	**Sockets, connectors**	**F**	**Douilles, connecteurs**
FG	Koax-Umrüstsatz	FG	Coaxial screw-in assembly	FG	Ensemble vissable coaxial
FH	Koax-Übergang auf Fremdsystem	FH	Coaxial adapter	FH	Adaptateur coaxial
FJ	BNC-Systemteil	FJ	BNC screw-in assembly	FJ	Ensemble vissable BNC
FK	Koaxial-UHF-Systemteil	FK	Coaxial UHF screw-in assembly	FK	Ensemble vissable coaxial UHF
FM	Mehrfachstecker, Buchsenleiste	FM	Multipoint connector	FM	Connecteur multiple
FN	Netz-Steckverbindung	FN	AC-supply connector	FN	Connecteur secteur
FO	Runde Mehrfach-Steckverbindung	FO	Round multipoint connector	FO	Connecteur multipoles rond
FP	Druckschalt-Steckverbindung	FP	Multipoint connector for PC boards	FP	Connecteur multipoles pour cartes imprimées
FR	Fassung für Lampe, Sicherung, usw.	FR	Socket for lamp, fuse, etc.	FR	Douille pour lampe, fusible etc. . . .
FT	Schwachstrom-Steckverbindung	FT	LV plug and socket	FT	Connecteur pour faible courant
FU	Hochspannungs-Steckverbindung	FU	HV plug and socket	FU	Connecteur pour haute tension
FV	Verbinder (z.B. AMP)	FV	Push-on connector	FV	Connecteur à enfichage
FZ	Zubehör für koax. Bauelemente	FZ	Accessories for coax. components	FZ	Accessoires pour composants coax.
H	**Software**	**H**	**Software**	**H**	**Logiciel**
HP	Software-Komponenten und Software-Module	HP	Rights to software components and software modules	HP	Droits d'utilisation de composants et modules logiciel
HS	Auf Informationsträger geladene Software	HS	Software data media	HS	Logiciel sur support d'information
J	**Meßinstrumente**	**J**	**Indicators**	**J**	**Indicateurs**
JD	Drehspul-Anzeigeinstrument	JD	Moving-coil meter	JD	Galvanomètre à cadre mobile
JE	Dreheisen-Anzeigeinstrument	JE	Moving-iron meter	JE	Galvanomètre à fer mobile
JF	Frequenzmesser	JF	Frequency meter	JF	Fréquencemètre
JG	Drehspulinstrument mit Gleichrichter	JG	Moving-coil meter with rectifier	JG	Galvanomètre à cadre mobile avec redresseur
JH	Betriebsstundenzähler	JH	Operating-hours counter	JH	Compteur d'heures de fonctionnement
JJ	Impulszähler	JJ	Pulse counter	JJ	Compteur d'impulsions
JK	Kleinst-Instrument, z.B. Abstimmanzeiger	JK	Mini-instrument, e.g. tuning indicator	JK	Petit indicateur, p.ex. indicateur d'accord
JM	Mechanisches Zählwerk	JM	Mechanical counter	JM	Compteur mécanique
JP	Projektions-Instrument (Leuchtziffer)	JP	Digital display	JP	Afficheur numérique
JQ	Quotientenmesser (Kreuzspulinstrum.)	JQ	Ratiometer (cross coul)	JQ	Quotientmètre (à cadres croisés)
JU	Uhrwerk	JU	Clockwork	JU	Mouvement d'horlogerie
JW	Elektrodyn. Anzeigeinstrument	JW	Electrodynamic meter	JW	Instrument électrodynamique
L	**Induktivitäten, Magnetik**	**L**	**Inductors, magnetic components**	**L**	**Composants inductifs et magnétiques**
LB	Blech- und Schnittbandkern mit Zubehör	LB	Laminated and C-cores with accessories	LB	Noyaux feuilletés et noyaux de type C, avec accessoires
LC	Keramische Spule	LC	Ceramic coil	LC	Bobine céramique
LD	Netz-, HF-Drossel, Df-Filter	LD	Choke, lead-through filter	LD	Self de choc, filtre de traversée
LE	Einzelkreis, Bandfilter	LE	Single tuned circuit, bandpass filter	LE	Circuit accordé, filtre passe-bande
LF	Ferritkern mit Zubehör	LF	Ferrite cores with accessories	LF	Noyaux en ferrite avec accessoires
LK	Karbonyleisenkern und elektrischer Kupferkern mit Zubehör	LK	Iron carbonyl slugs and copper slugs with accessories	LK	Noyaux en fer carbonyle et en cuivre, avec accessoires
LL	Luftspule	LL	Air-core coils	LL	Bobines à air
LM	Magnetband und -platte	LM	Magnetic tapes and disks	LM	Bandes et disques magnétiques
LS	Schirmbecher	LS	Screening cans	LS	Boîtiers de blindage
LT	Netztransformator	LT	Power transformer	LT	Transformateur secteur
LU	NF-Übertrager	LU	AF transformer	LU	Transformateur BF
LV	Variometer	LV	Variometer	LV	Variomètre
LW	Wickelkörper, allgemein	LW	Coil formers, general	LW	Carcasses de bobine, en général

ROHDE&SCHWARZ

Zusammenstellung der lieferbaren Netzkabel
List of power cables available
Liste des câbles d'alimentation disponibles

Sach-Nr. Stock No. Référence	Schutzkontaktstecker nach: Earthed-contact connector: Fiche à contact de protection:	Vorzugsweise verwendet in: Preferably used in: Utilisé de préférence en:
DS 006.7013	BS 1363: 1967' 13A entspr. IEC 83: 1975 Standard B2 BS 1363: 1967' 13A complying with IEC 83: 1975 Standard B2 BS 1363: 1967' 13A suivant CEI 83: 1975 norme B2	Großbritanien Great Britain Grande-Bretagne
DS 006.7020	Typ 12 nach SEV-Vorschrift 1011.1059, Normblatt S 24 507 Type 12 complying with SEV regulation 1011.1059, standard sheet S 24 507 Type 12 suivant la norme SEV 1011.1059, feuille S 24 507	Schweiz Switzerland Suisse
DS 006.7036	Typ 498/13 nach USA-Vorschrift UL 498, bzw. IEC 83 Type 498/13 complying with US regulation UL 498 or with IEC 83 Type 498/13 suivant la norme E.U.A. UL 498 ou la norme CEI 83	USA / Kanada USA / Canada E.U.A. / Canada
DS 006.7107	Typ SAA3 10 A, 250 V, nach AS C112-1964 Ap. Type SAA3 10 A, 250 V, complying with AS C112-1964 Ap. Type SAA3 10 A, 250 V, suivant AS C112-1964 Ap.	Australien Australia Australie
DS 025.2365	DIN 49 441, 10 A, 250 V	Europa (ohne Schweiz) Europe (Switzerland not included) Europe (Suisse non comprise)

Cross-Reference List of Class Designation Letters

IEC Publication 113-2 (1971) Item Designations, Letter Codes
ANSI Y32.2-1975 (IEEE Std 315-1975), Section 22, Class Designation Letters

Note: The designation letters used in the R&S Manuals correspond to the letter codes of the IEC Standard identified in the first column!

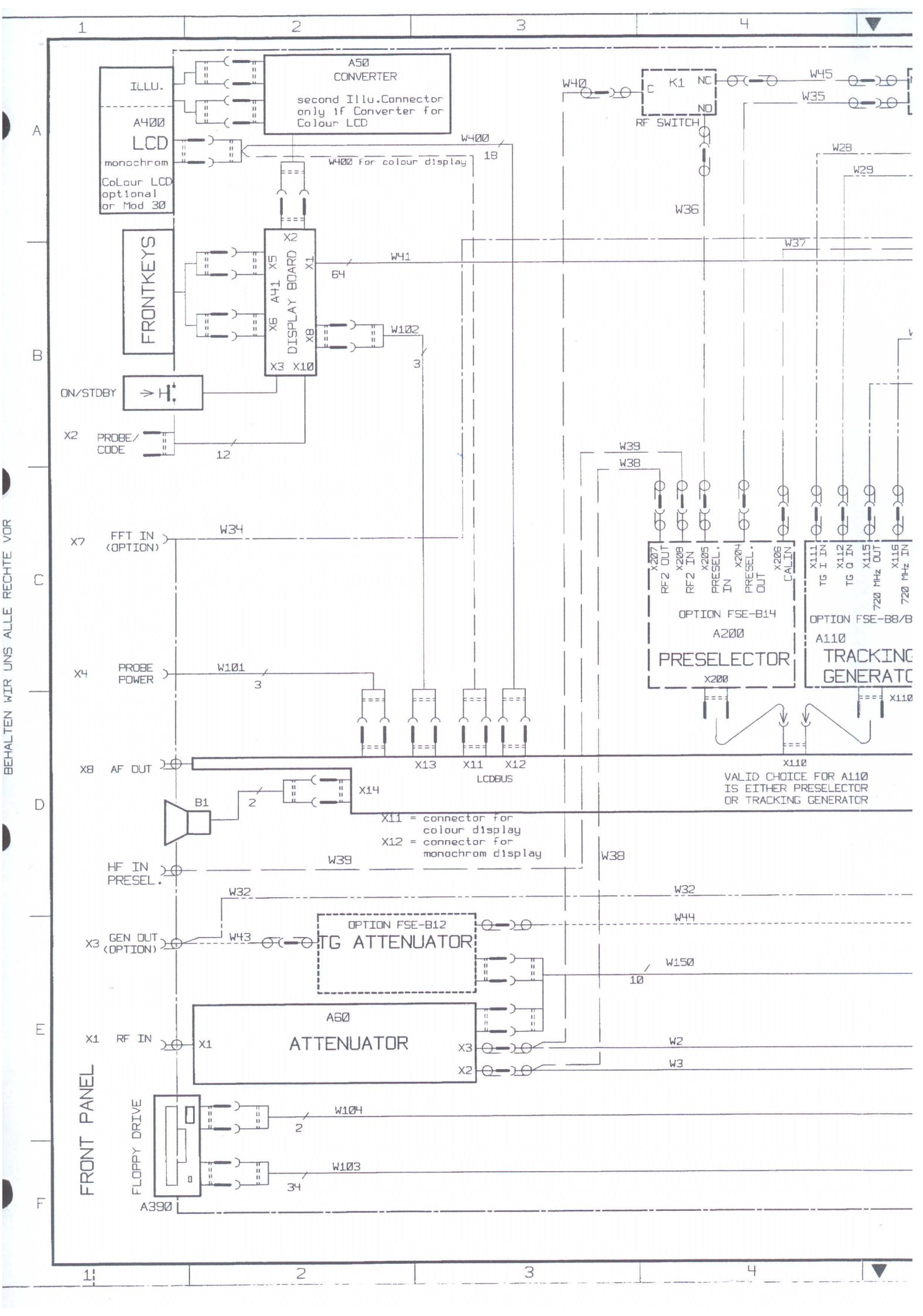
IEC Publication 113-2 Terminology	Letter Code IEC	Y32.2
Acoustical indicator	H	LS
Adjustable resistor	R	R
Aerial	W	E
Amplifier	A	AR
Amplifier (with tubes)	A	AR
Arrester	F	E
Assemblies	A	A,U
Auxiliary switch	S	S
Battery	G	BT
Bistable element	D	U,A
Brake	Y	MP
Busbar	W	W
Cable	W	W
Cable balancing network	Z	Z
Capacitor	C	C
Changer	U	A,B,G,MT
Circuit breaker	Q	CB
Clutch	Y	MP
Coder	U	U,A
Compander	Z	A
Connecting stage	S	S
Contactors	K	K
Control switch	S	S
Converter	U	A,U,MG
Core, storage	D	E
Crystal filter	Z	FL
Crystal transducer	B	Y
Current transformer	T	T
Delay device	D	DL
Delay line	D	DL
Demodulator	U	A
Dial contact	S	S
Diode	V	D
Dipole	W	E
Disconnecting plug	X	P
Disconnecting socket	X	X
Discriminator	U	A
Disk recorder	D	A
Dynamotor	B	MG
Electrically operated mechanical device	Y	MT
Electronic tube	V	V
Equalizer	Z	EQ
Filter	Z	FL
Frequency changer	U	A,B,G
Fuse	F	F
Gas discharge tube	V	V
Generator	G	G
Heating device	E	HR
Hybrid	Z	Z
Indicating device	P	DS
Induction coil	L	L
Inductors	L	L
Integrating measuring device	P	M,MT,Z
Inverter	U	A,U,PS,MG
Isolator	Q	A
Jumper wire	W	W
Laser	A	MT,A
Lighting device	E	DS
Limit switch	S	S
Limiter	Z	MT,RE
Line trap	L	FL,MP,V
Loudspeaker	B	LS
Magnetic amplifier	A	AR

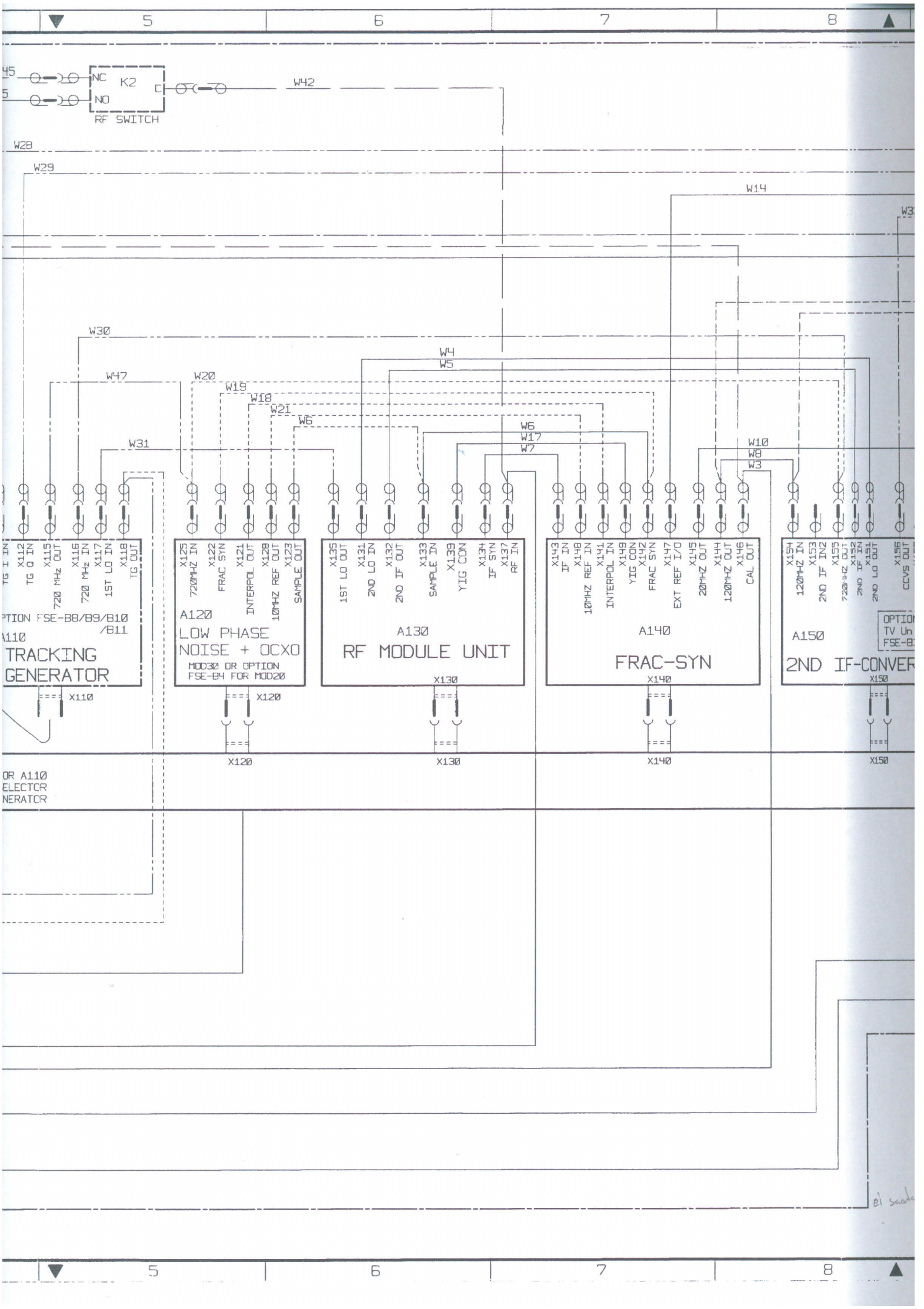
IEC Publication 113-2 Terminology	Letter Code IEC	Y32.2
Magnetic tape recorder	D	A
Maser	A	A
Measuring equipment	P	M
Microphone	B	MK
Miscellaneous	E	E
Modulator	U	A
Monostable element	D	A,U
Motor	M	B
Optical indicator	H	DS
Oscillator	G	Y,G
Overvoltage discharge device	F	F,E
Parabolic aerial	W	E
Photoelectric cell	B	V
Pickup	B	PU
Plug	X	P
Pneumatic valve	Y	MP
Potentiometer	R	R
Power switchgear	Q	CB,S
Protective device	F	F
Pushbutton	S	S
Quartz-oscillator	G	Y
Recording device	P	A,M
Register	D	A,U,M
Relay	K	K
Resistor	R	R
Resolver	B	B
Rheostat	R	R
Rotating frequency generator	G	G,MG
Rotating generator	G	G
Selector	S	S
Selector switch	S	S
Semiconductor	V	D,CR,Q
Shunt (resistor)	R	R
Signal generator	P	A
Signaling device	H	DS
Socket	X	X
Soldering terminal strip	X	E,TB
Static frequency changer	U	A
Storage device	D	A,U
Subassembly	A	A
Supply	G	A,PS
Supply device	G	A,PS
Synchro	B	B
Telegraph translator	U	A
Terminal	X	E
Terminal board	X	TB
Termination	Z	AT
Test jack	X	E,J
Testing equipment	P	A
Thermistor	R	RT
Thermo cell	B	A,TC
Thermoelectric sensor	B	A
Thyristor	V	Q
Transducer (nonelectrical quantity to electrical quantity)	B	A,BT
Transformer	T	T
Transmission path	W	W
Transistor	V	Q
Tube (electron)	V	V
Voltage transformer (potential)	T	T
Waveguide	W	W
Waveguide directional coupler	W	DC

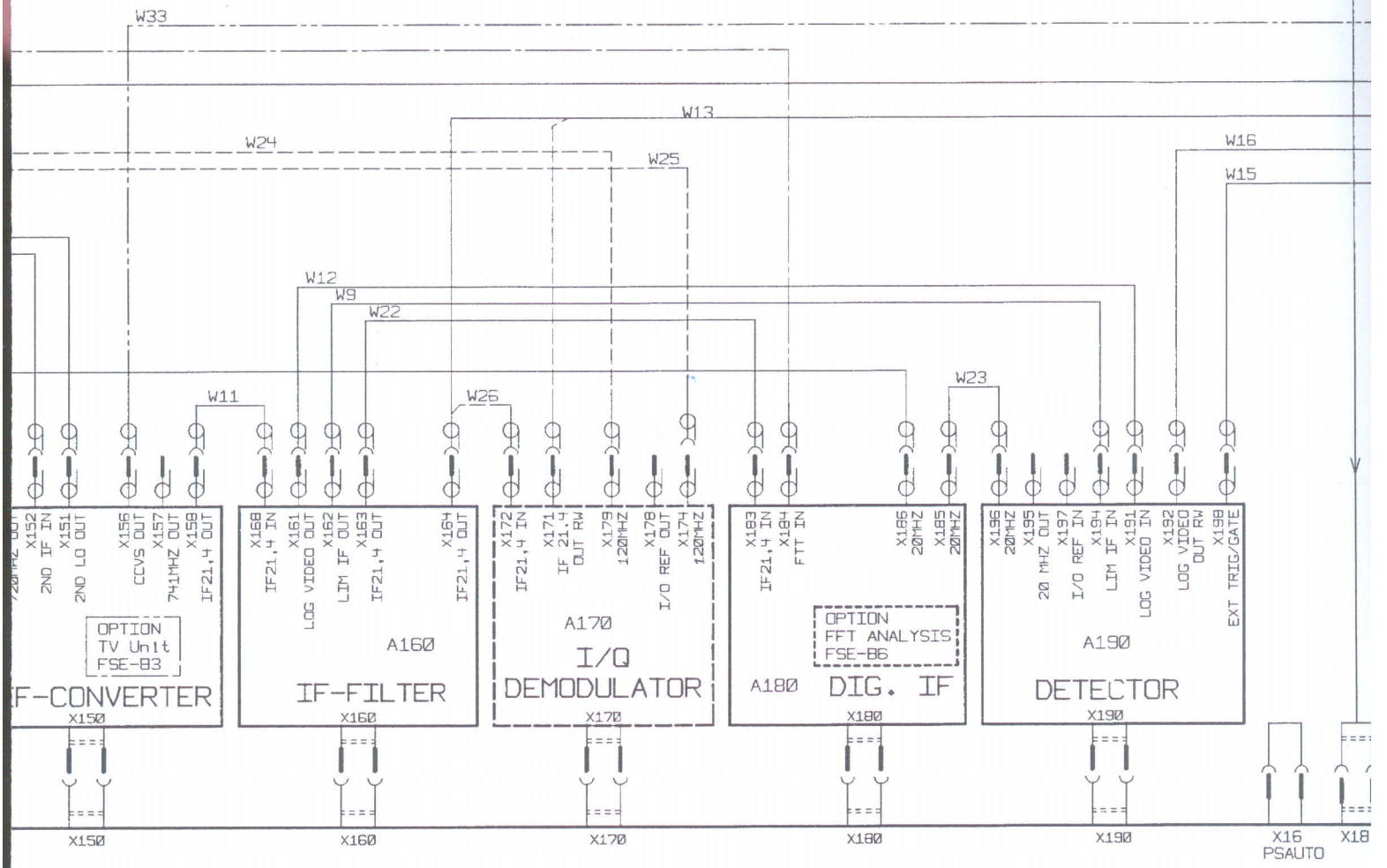
ROHDE&SCHWARZ

Stromläufe
Bestückungspläne
Circuit diagrams
Components plans
Schémas de circuit
Plans des composants

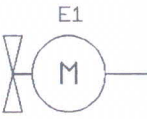
(R 29500 Bl. 4)
095.1000 Bl. 4




5
6
7
8
K2
NC
NO
C
RF SWITCH
W42
W28
W29
W14
W30
W4
W5
W47
W20
W19
W18
W21
W6
W17
W7
W10
W8
W3
W31
X112
TG Q IN
X115
720 MHz OUT
X116
720 MHz IN
X117
1ST LO IN
X118
TG OUT
TRACKING GENERATOR
X110
X125
720MHZ IN
X122
FRAC SYN
X121
INTERPOL OUT
X128
10MHZ REF OUT
X123
SAMPLE OUT
A120
LOW PHASE NOISE + OCXO
MOD30 OR OPTION FSE-B4 FOR MOD20
X120
X135
1ST LO OUT
X131
2ND LO IN
X132
2ND IF OUT
X133
SAMPLE IN
X139
YIG CON
X134
IF SYN
X137
RF IN
A130
RF MODULE UNIT
X130
X143
IF IN
X148
10MHZ REF IN
X141
INTERPOL IN
X149
YIG CON
X142
FRAC SYN
X147
EXT REF I/O
X145
20MHZ OUT
X144
120MHZ OUT
X146
CAL OUT
A140
FRAC-SYN
X140
X154
120MHZ IN
X153
2ND IF IN2
X155
720MHZ OUT
X152
2ND IF IN
X151
2ND LO OUT
X156
CCVS OUT
A150
2ND IF-CONVER
X150
X120
X130
X140
X150



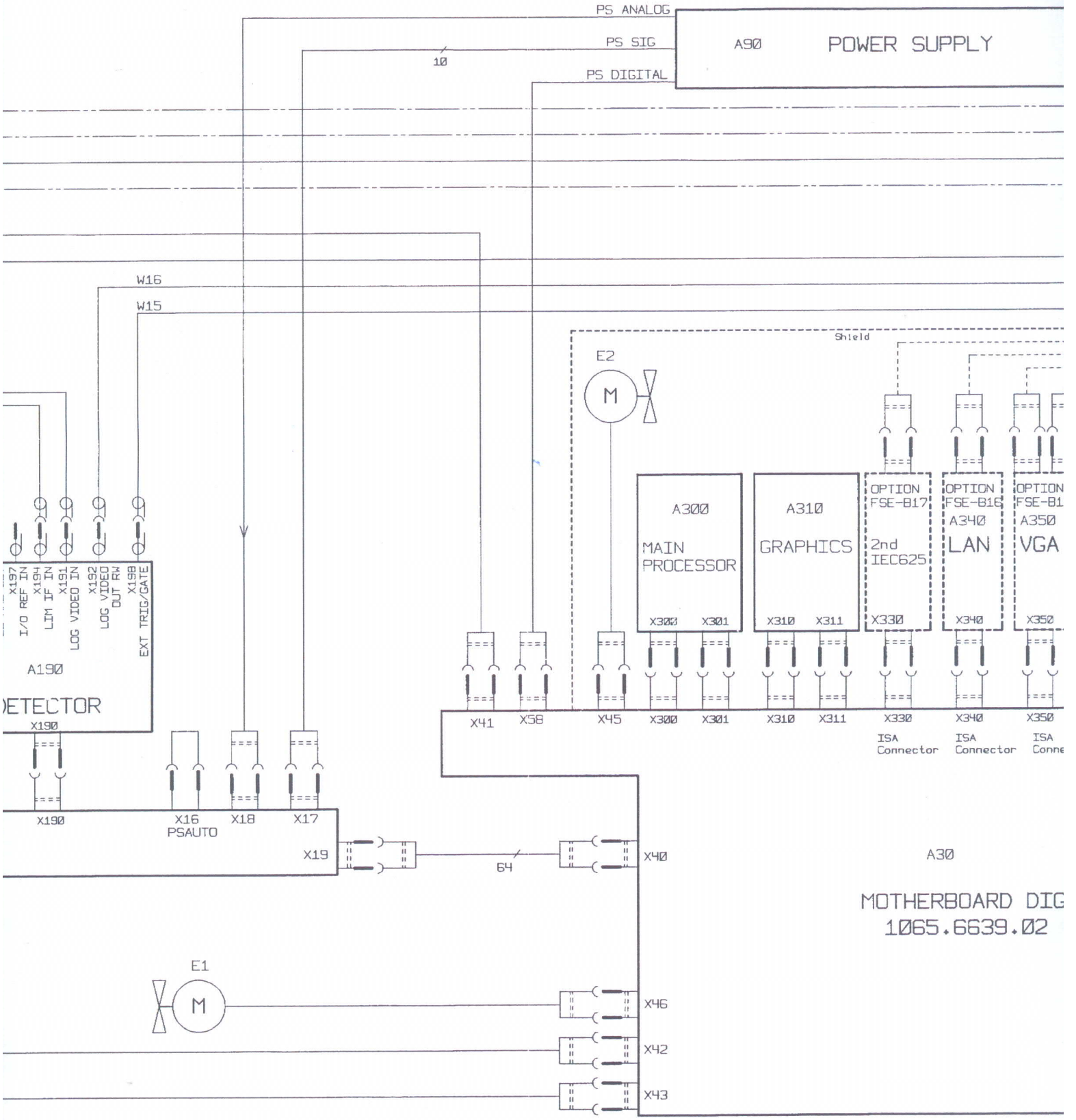
A10 MOTHERBOARD 1065.6516.02



Options

FSE-B1 Colour Display (for MOD 20)
FSE-B2 Frequency Extension 7 GHz for FSEA 20/30
FSE-B3 TV Demodulator
FSE-B4 Low Phase Noise
FSE-B5 Digital IF Filter (1 Hz ... 1 KHz) for FSEA 20
FSE-B6 FFT Analysis
FSE-B7 Vector Analysis
FSE-B8 Tracking Generator
FSE-B9 Tracking Generator with I/Q modulisable
FSE-B12 Attenuator for Tracking Generator
FSE-B13 EMI Detector
FSE-B14 Preselector and 10dB Preamp
FSE-B15 Computer Function
FSE-B16 LAN Interface
FSE-B17 2nd IEC625 for FSE-B15

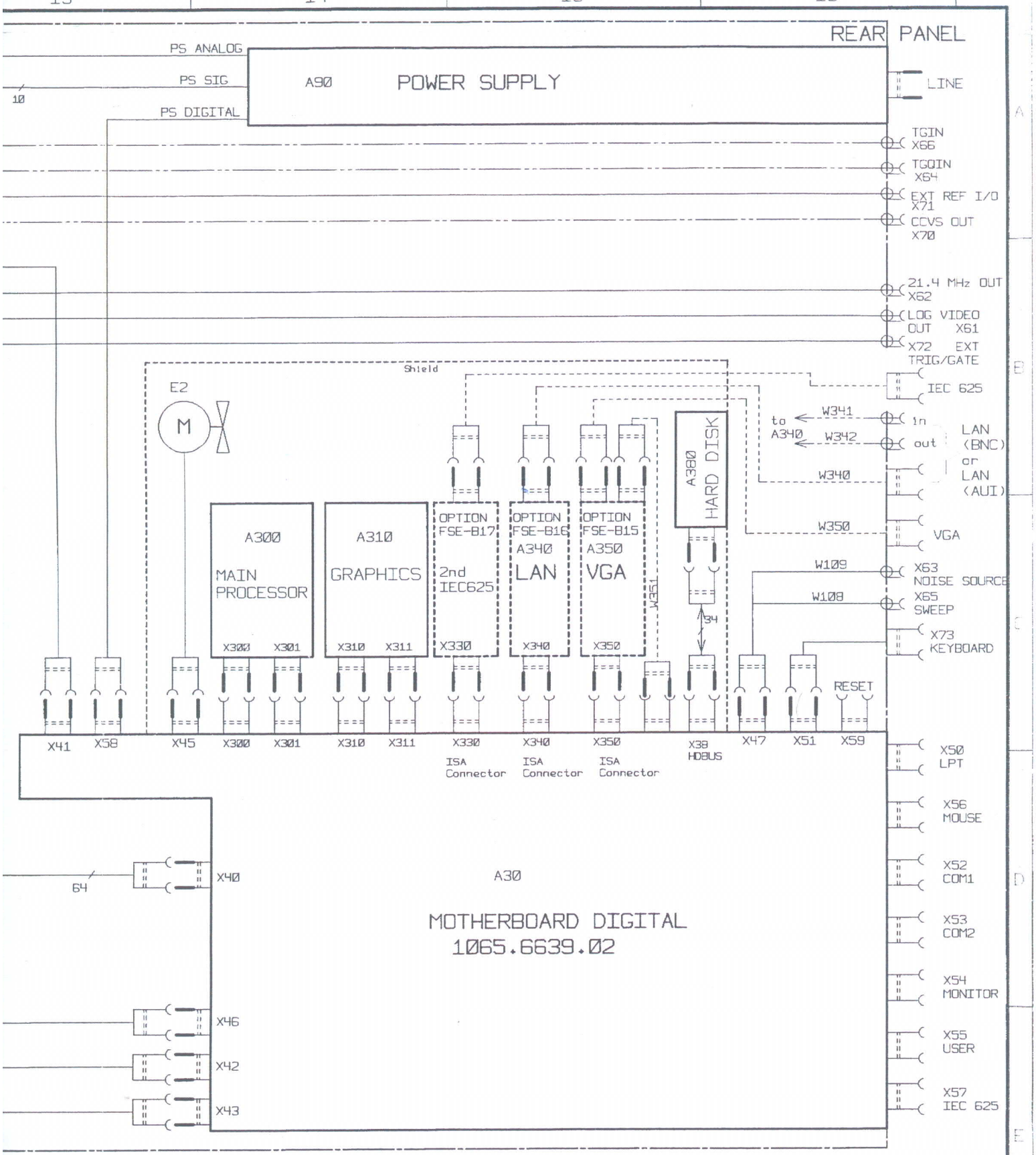
ei saatavissa



Versions

MOD 20 = FSEA 20: MODEL WITH MONOCHROM DISPLAY
MOD 30 = FSEA 30: MODEL WITH COLOUR DISPLAY AND LC

01/02		25.04.95	Pf	1ESK	TAG	NAME	BENE
				BEARB.	12.94	Pfeil	GG
				GEPR.			
				NORM			
				PLOTT			
							ZEIC
							10E
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ROHDE&SCHWARZ			
				ZU GERAET FSEA			REG.I.



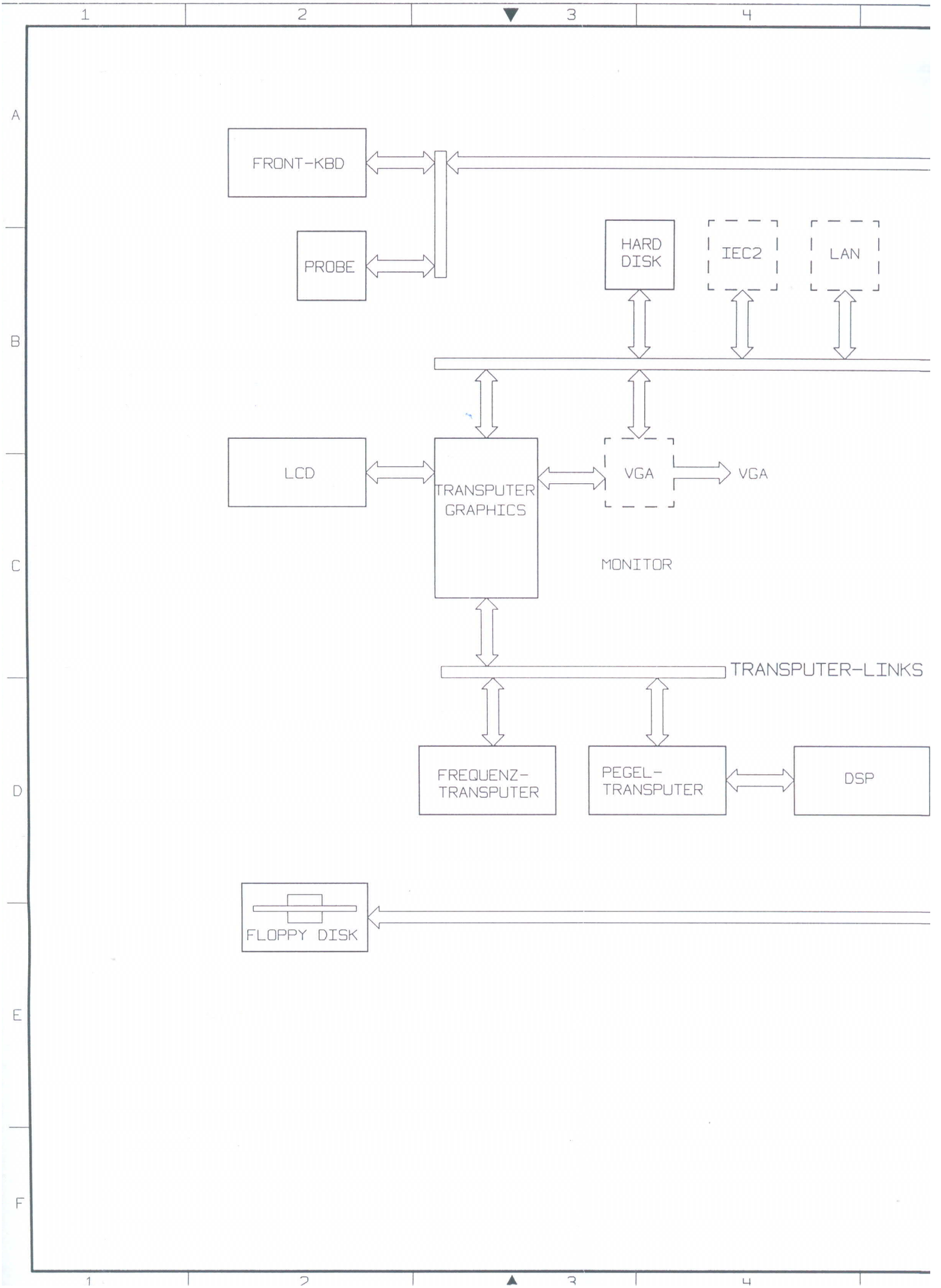
Versions

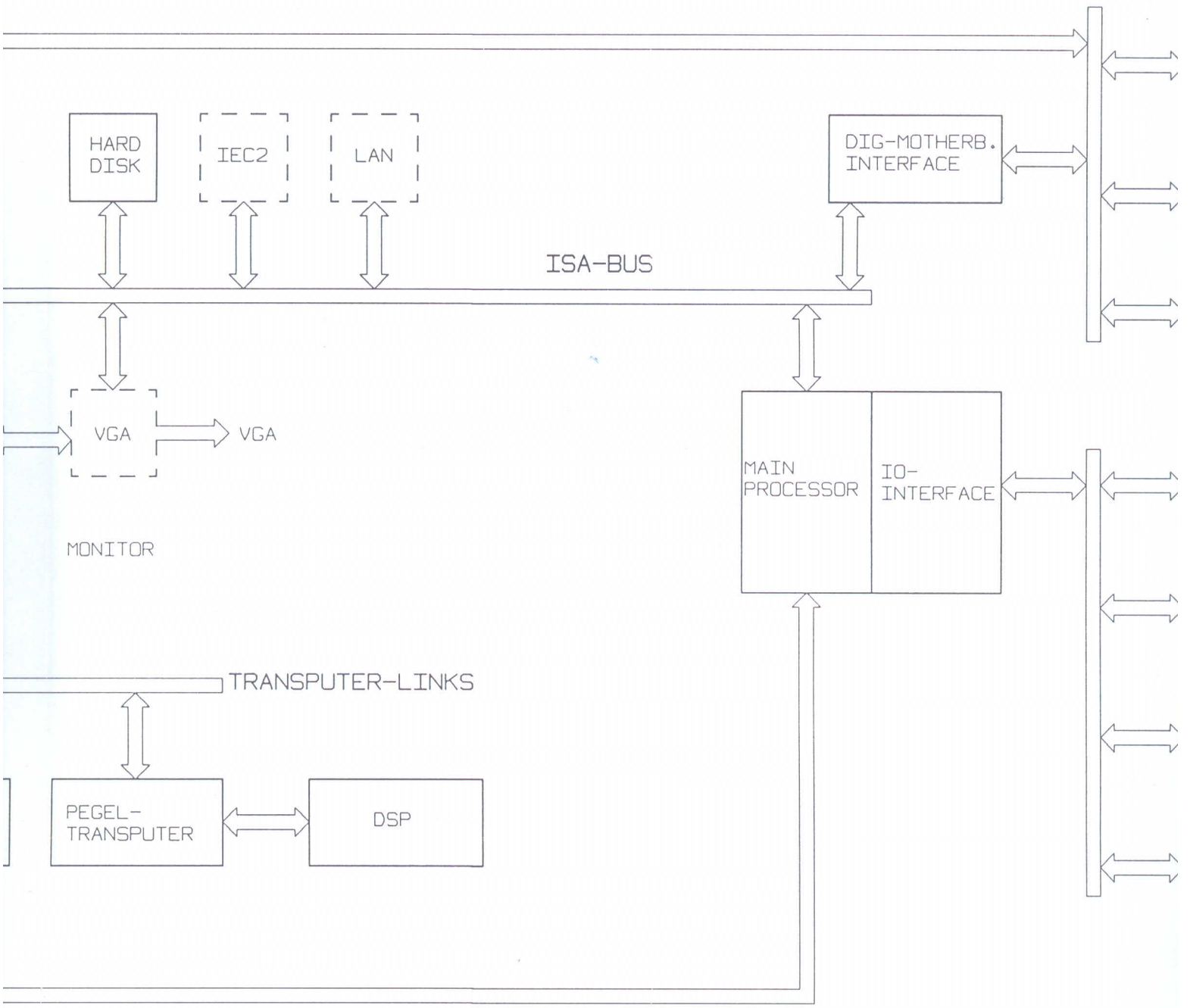
MOD 20 = FSEA 20: MODEL WITH MONOCHROM DISPLAY
MOD 30 = FSEA 30: MODEL WITH COLOUR DISPLAY AND LOW PHASE NOISE

01/02		25.04.95	Pf	1ESK	TAG	NAME	BENENNUNG
				BEARB.	12.94	Pfeil	GG FSEA 20/30
				GEPR.			
				NORM			
				PLOTT			
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ROHDE&SCHWARZ			ZEICHN.-NR. 1065.6000.01 S
				ZU GERAET FSEA			REG.I.V. 1065.6000 V

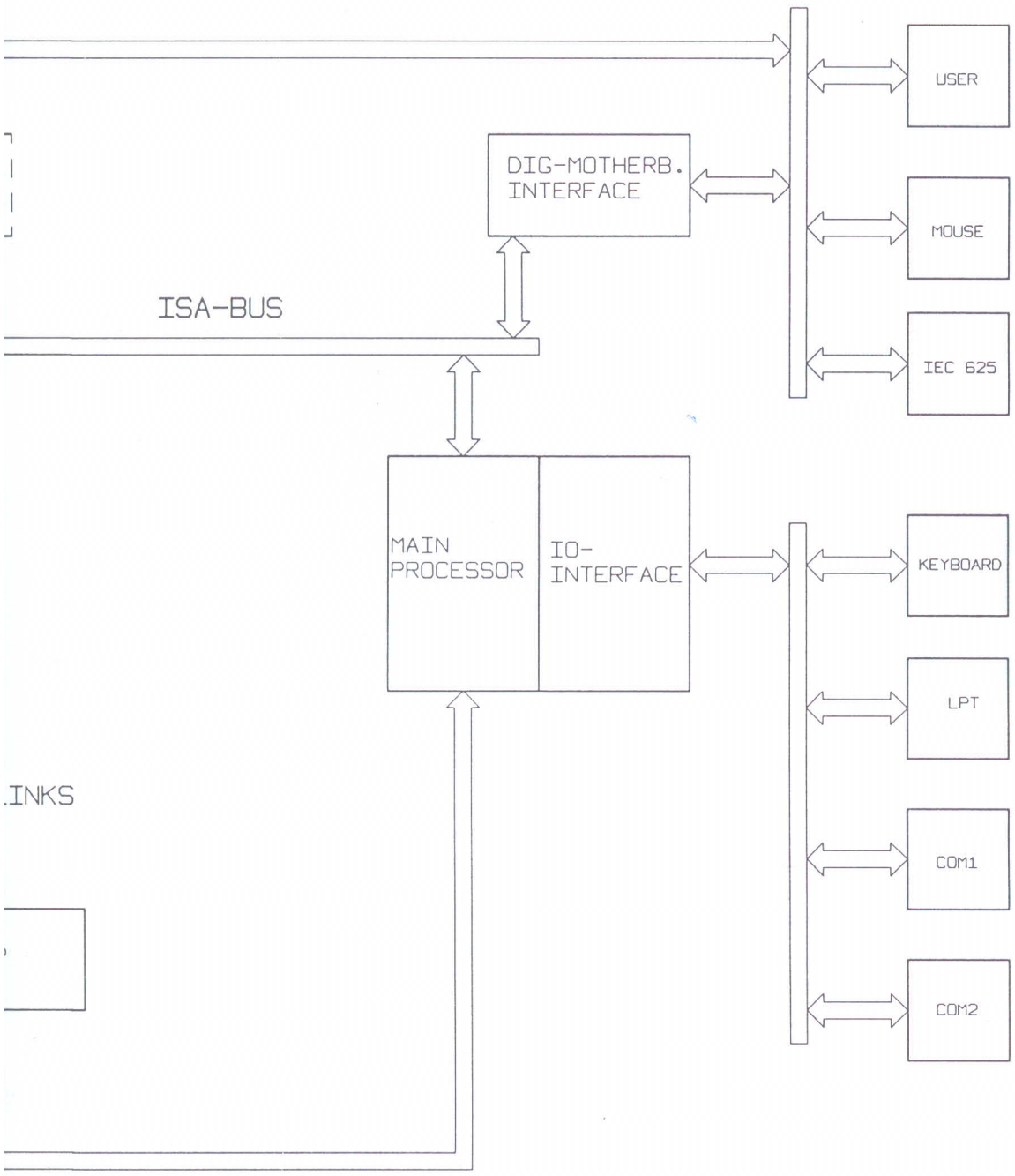
BLATT-NR. 1 V. 5 BL.

ERSTE Z.


FRONT-KBD
PROBE
HARD DISK
IEC2
LAN
LCD
TRANSPUTER GRAPHICS
VGA
VGA
MONITOR
TRANSPUTER-LINKS
FREQUENZ-TRANSPUTER
PEGEL-TRANSPUTER
DSP
FLOPPY DISK



01/02		25.04.95	Pf	1ESK	TAG	NAME	BENENNUNG
				BEARB.	12.94	Pfeil	GG F
				GEPR.			
				NORM			
				PLOTT	26.04.95		top
				R/S ROHDE&SCHWARZ			ZEICHN.-NR 1065.6
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ZU GERAET FSEA			REG.I.V. 10



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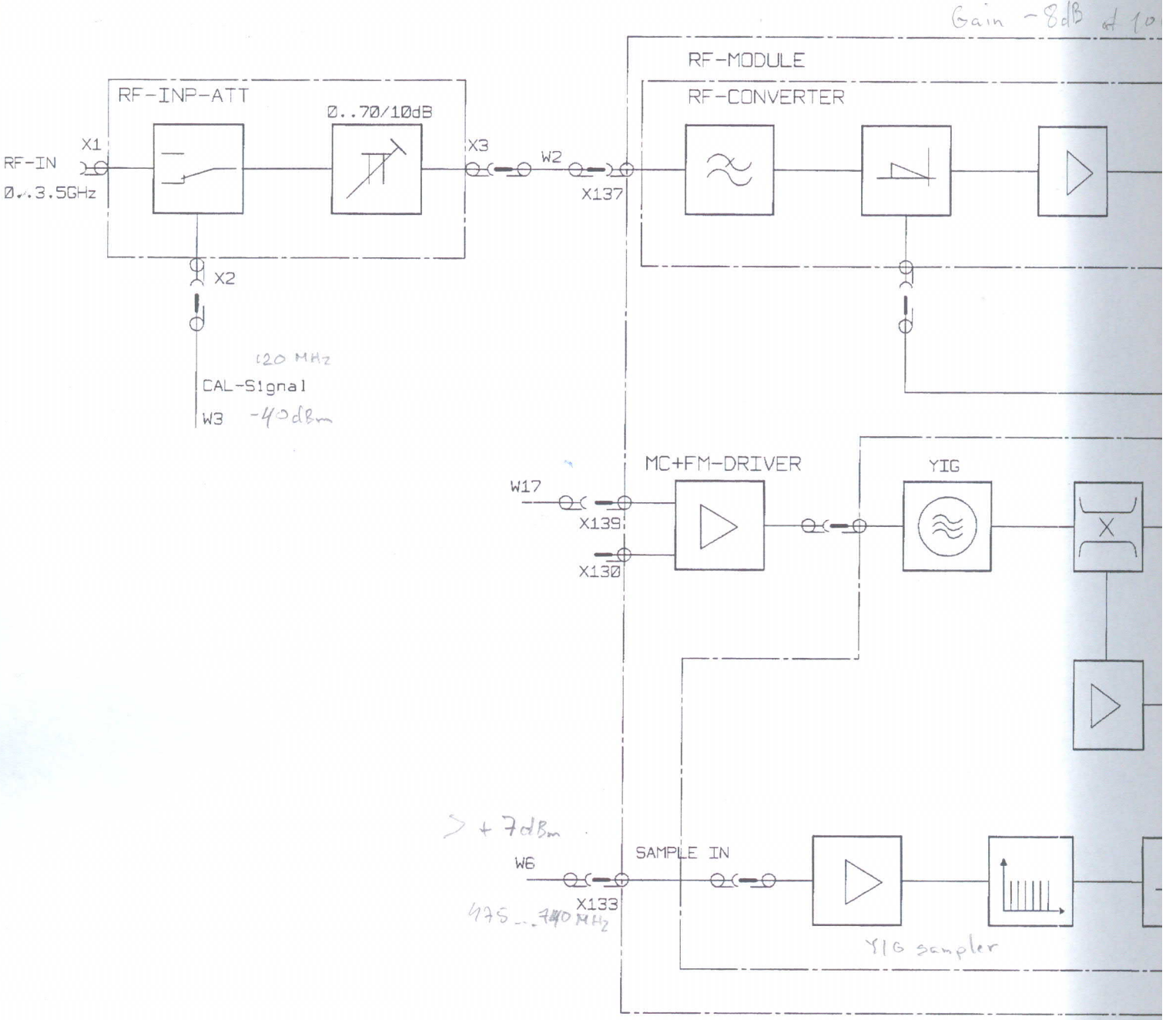
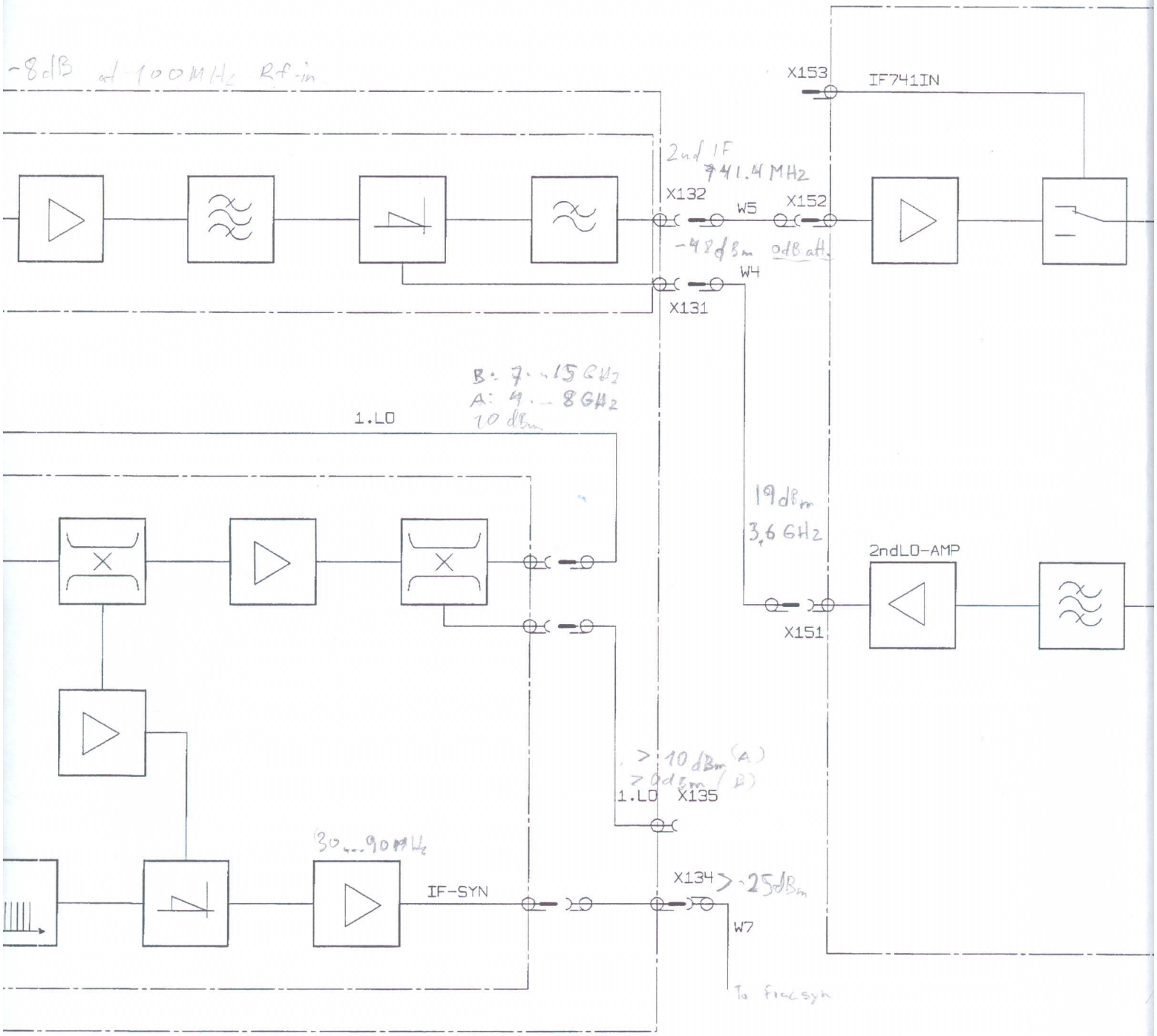
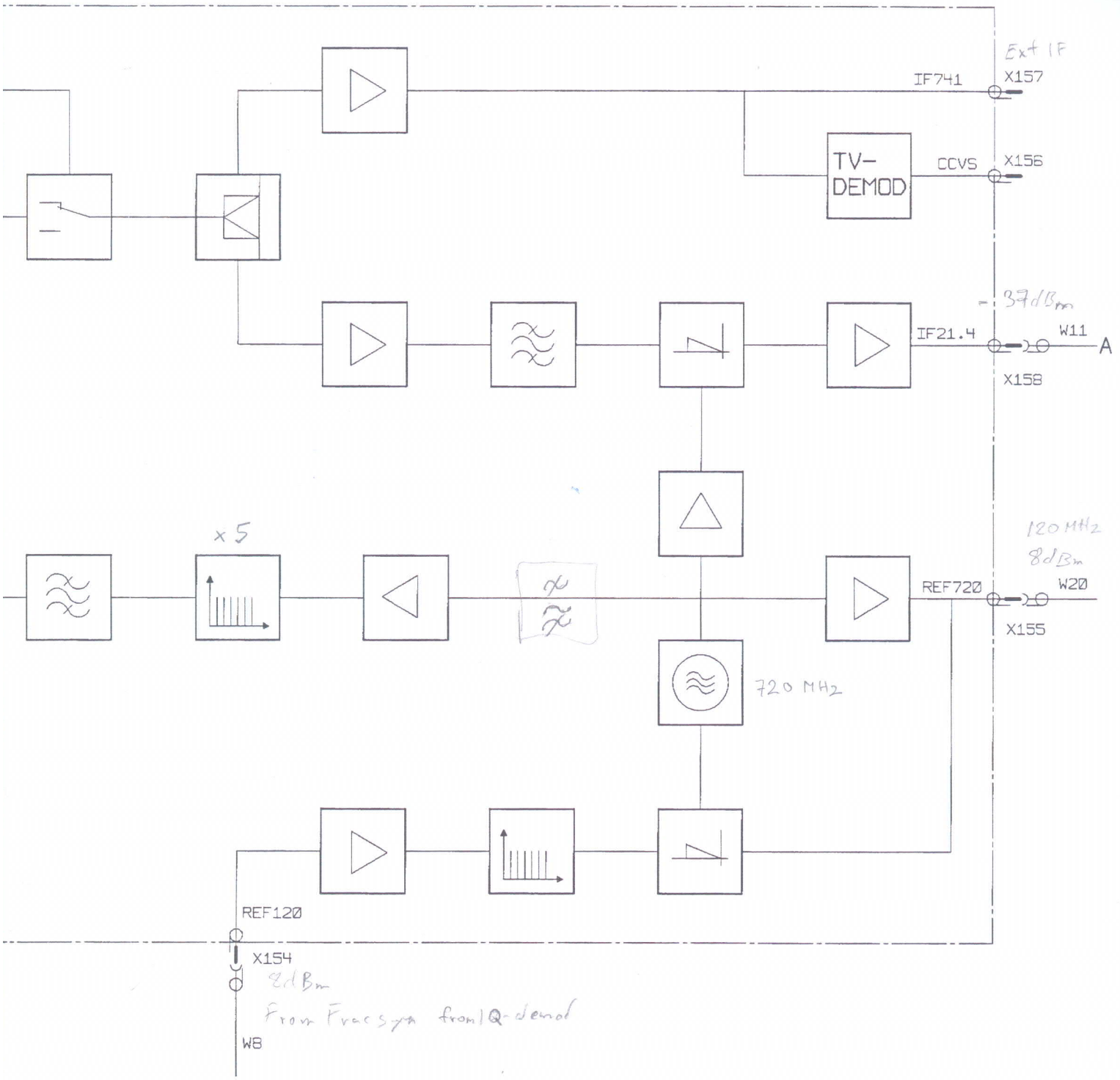
				BEARB.	12.94	Pfeil	GG FSEA 20/30
				GEPR.			
				NORM			
				PLOTT	26.04.95		top sheet1
				ROHDE&SCHWARZ			ZEICHN.-NR. 1065.6000.01 S BLATT-NR. 2
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ZU GERAET FSEA			REG.I.V. 1065.6000 V ERSTE Z. v. 5 BL.


Gain -8dB
RF-MODULE
RF-CONVERTER
RF-INP-ATT
Ø..70/10dB
RF-IN
Ø..3.5GHz
X1
X3
W2
X137
X2
120 MHz
CAL-Signal
W3 -40dBm
MC+FM-DRIVER
YIG
W17
X139
X130
> +7dBm
SAMPLE IN
W6
X133
475 ... 740 MHz
YIG sampler



ACHTUNG: EGB!
ELEKTROSTATISCH GEFAEHRDETE BAUELEMENTE ERFORDERN EINE BESONDERE HANDHABUNG.
ATTENTION ESD!
ELECTROSTATIC SENSITIVE DEVICES REQUIRE A SPECIAL HANDLING



01/02		25.04.95	Pf	1ESK	TAG	NAME	BENENNUNG
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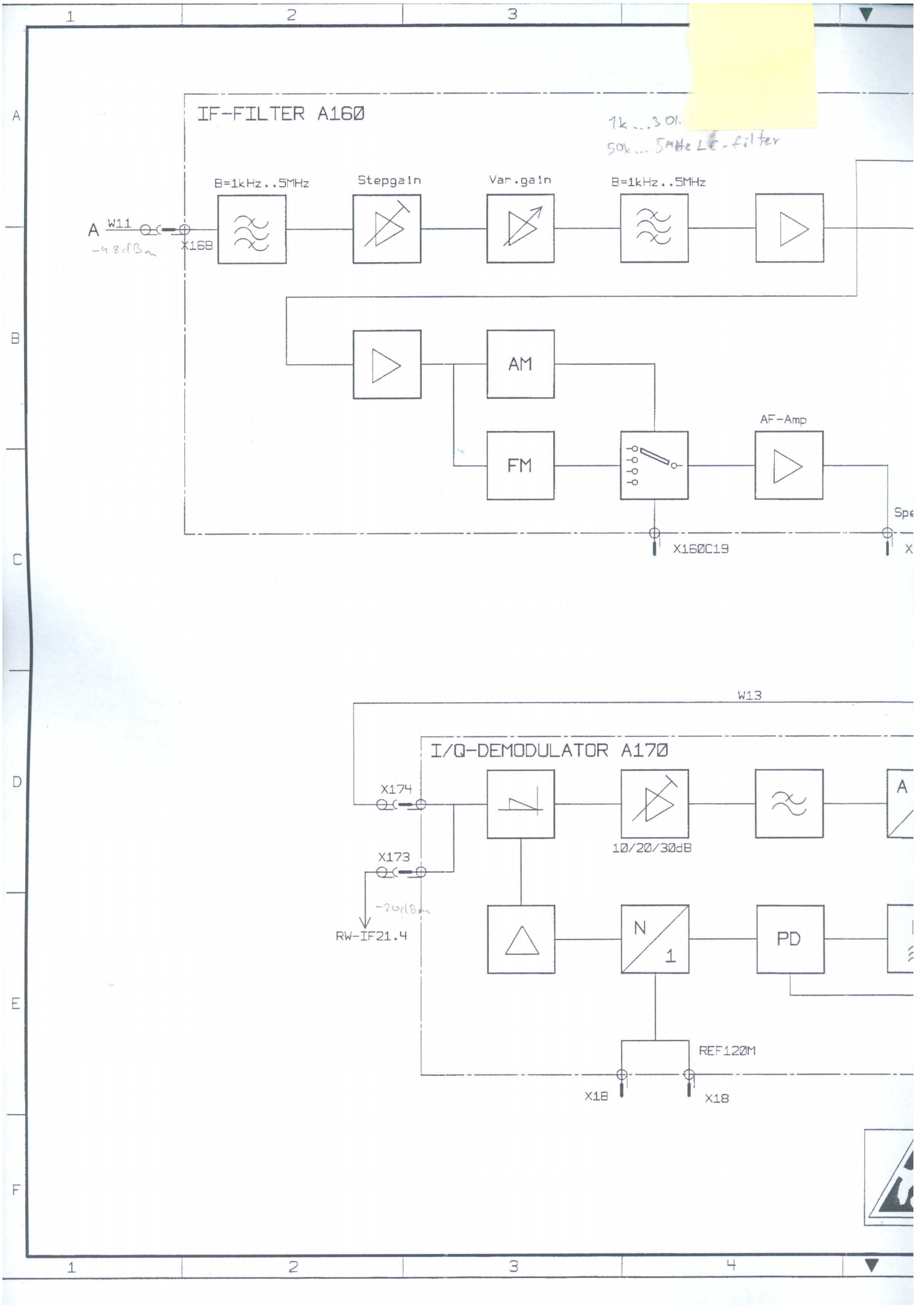
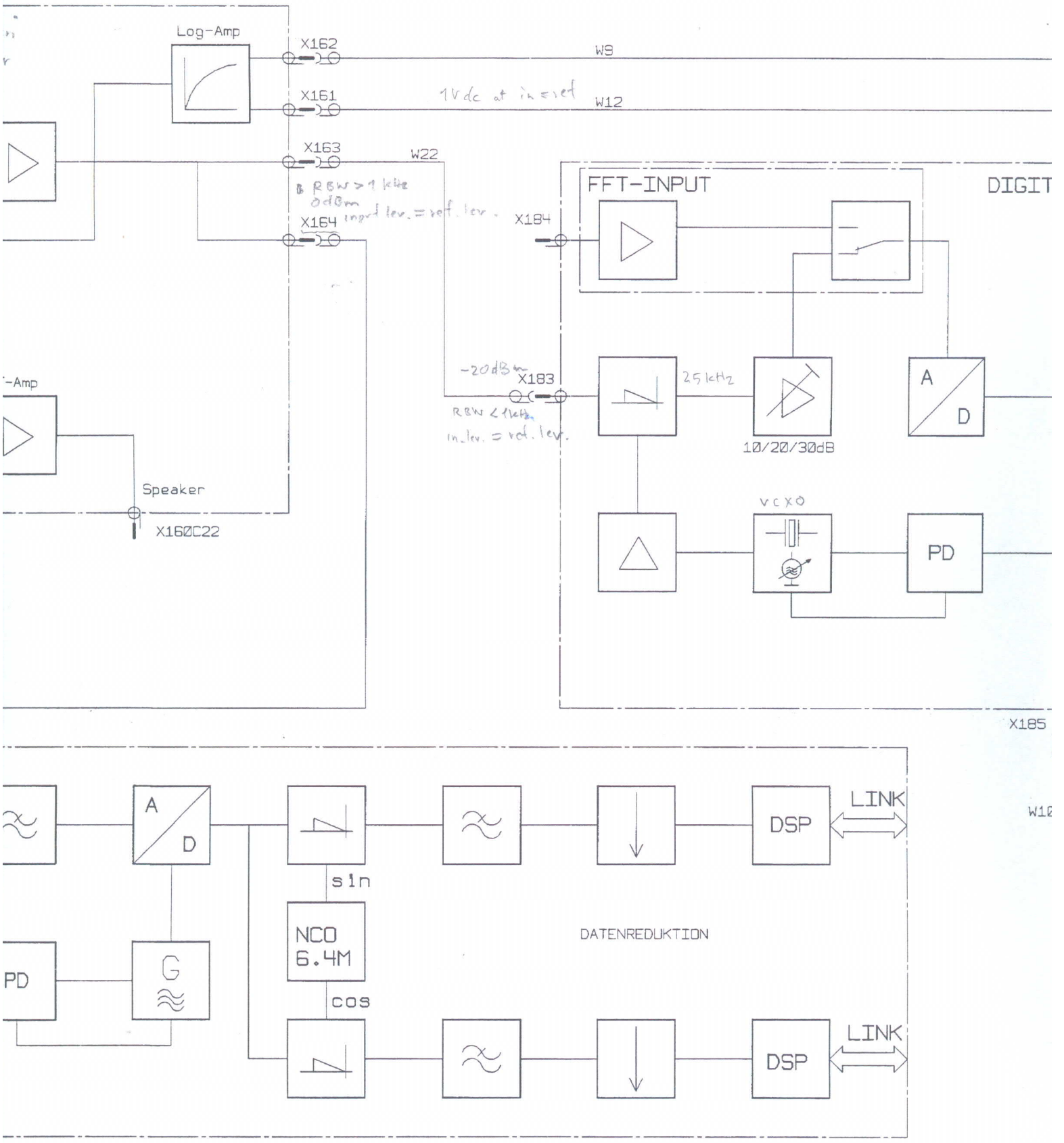
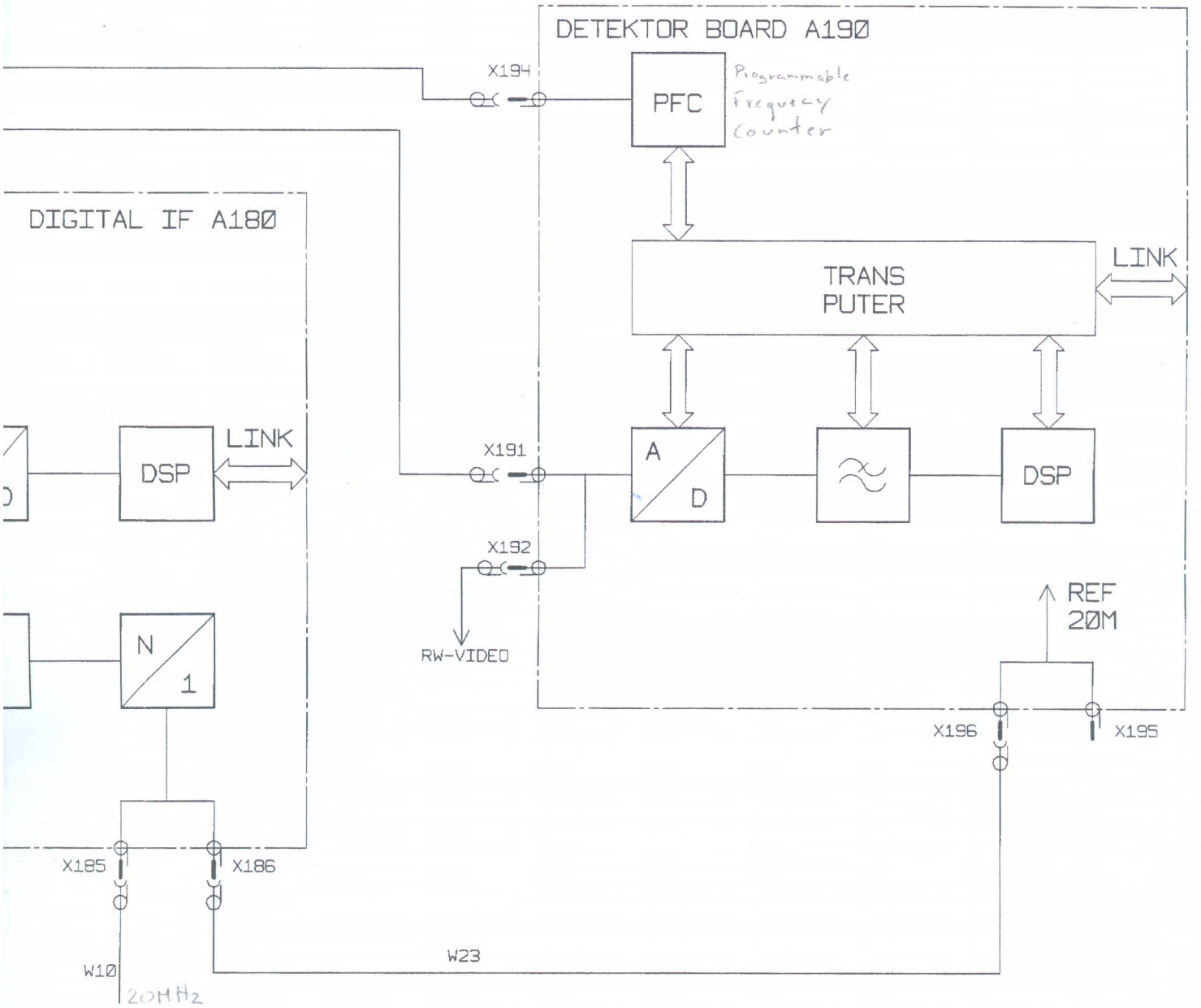
				GEPR.			
				NORM			
				PLOTT	26.04.95		top sheet2
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ROHDE&SCHWARZ			ZEICHN.-NR. 1065.6000.01 S
				ZU GERAET FSEA			REG.I.V. 1065.6000 V

BLATT-NR. 3
V. 5 BL.
ERSTE Z.


IF-FILTER A160
1k ... 30k
50k ... 5MHz LC-filter
B=1kHz..5MHz
Stepgain
Var.gain
B=1kHz..5MHz
A
W11
-48dBm
X168
AM
FM
AF-Amp
X160C19
W13
I/Q-DEMODULATOR A170
X174
X173
-20dBm
RW-IF21.4
10/20/30dB
N
1
PD
REF120M
X18
X18



ACHTUNG: EGB!
ELEKTROSTATISCH GEFAEHRDETE
BAUELEMENTE ERFORDERN EINE
BESONDERE HANDHABUNG.
ATTENTION ESD!
ELECTROSTATIC SENSITIVE DEVICES
REQUIRE A SPECIAL HANDLING



01/02		25.04.95	Pf	1ESK	TAG	NAME	BENENNUNG
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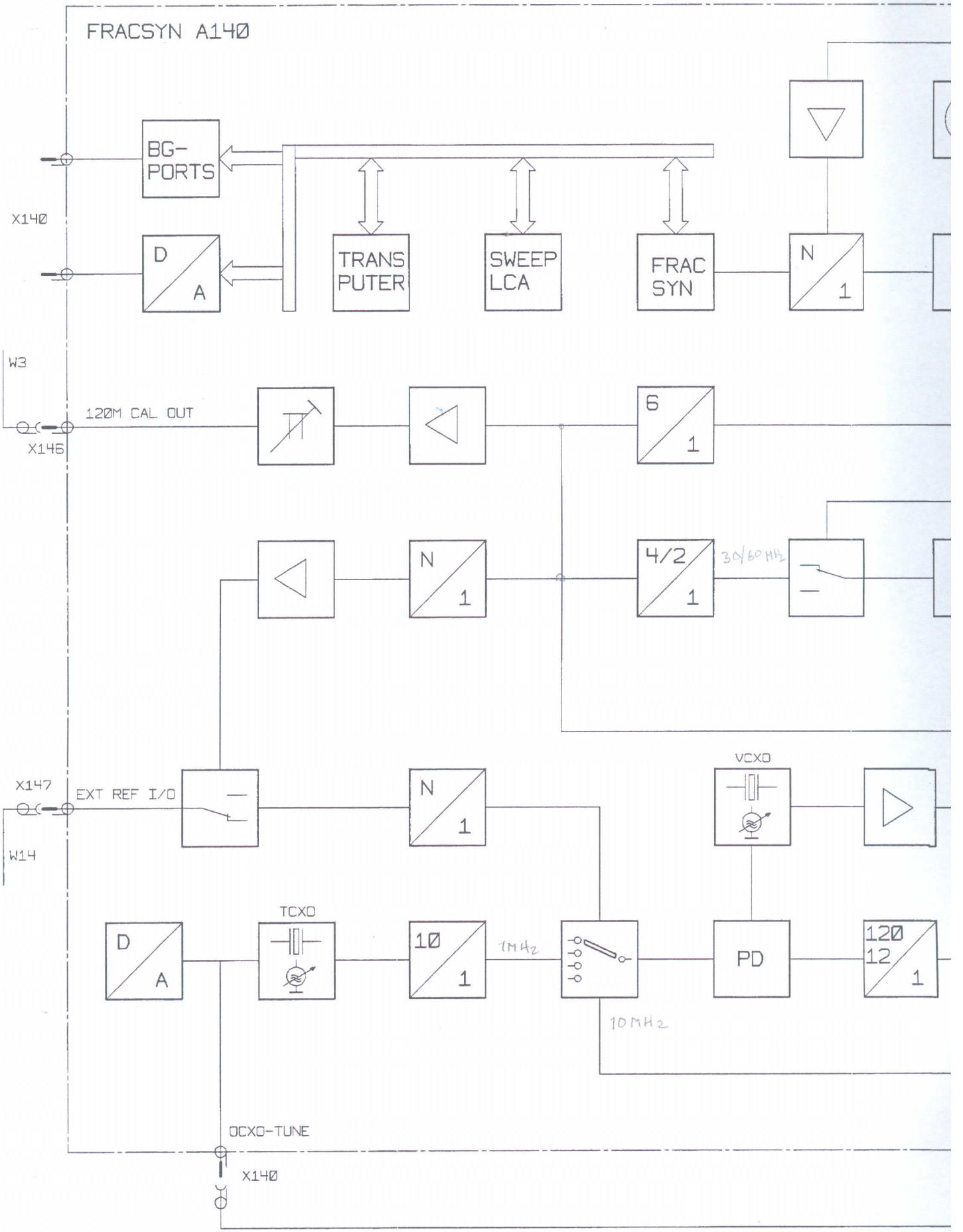
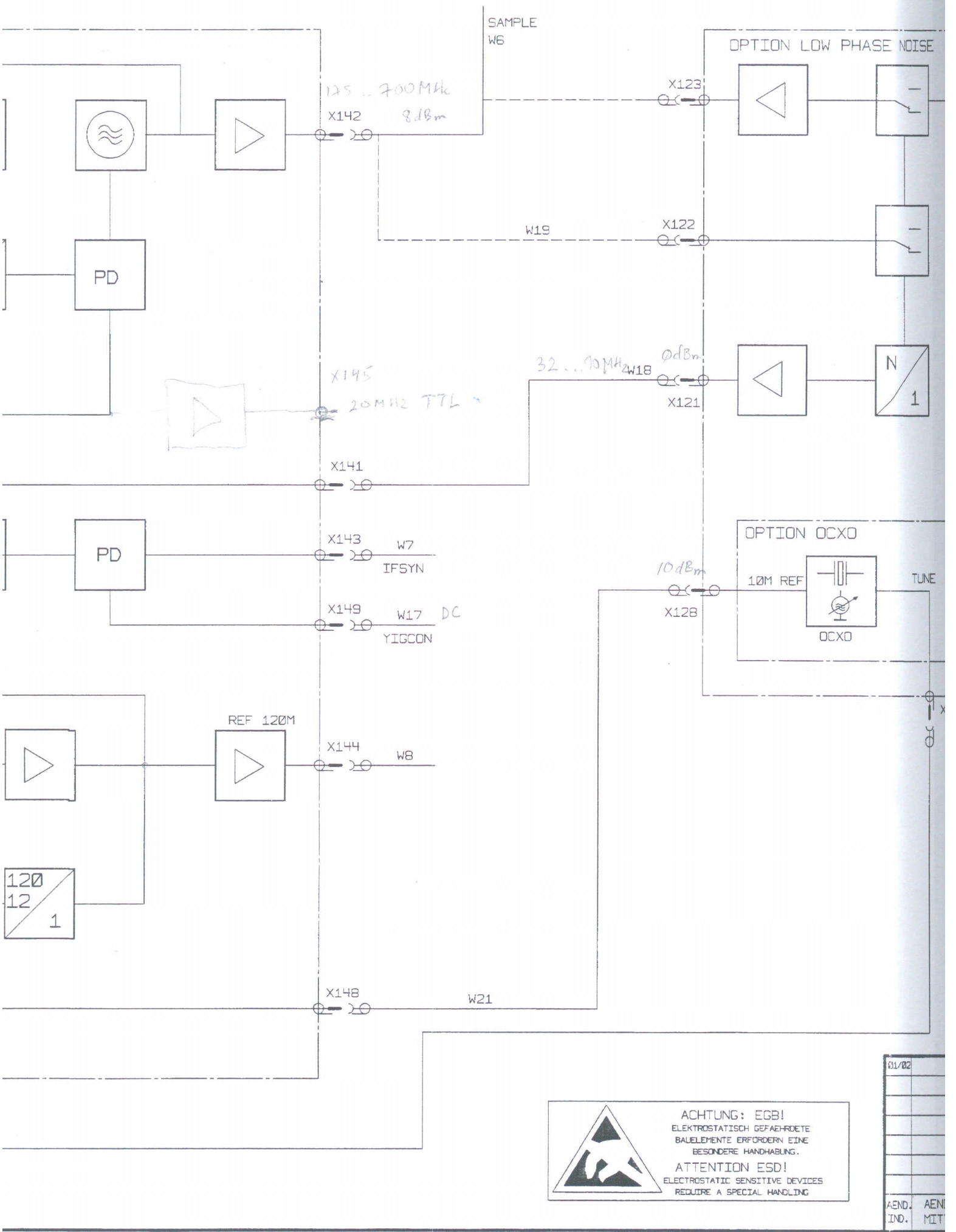
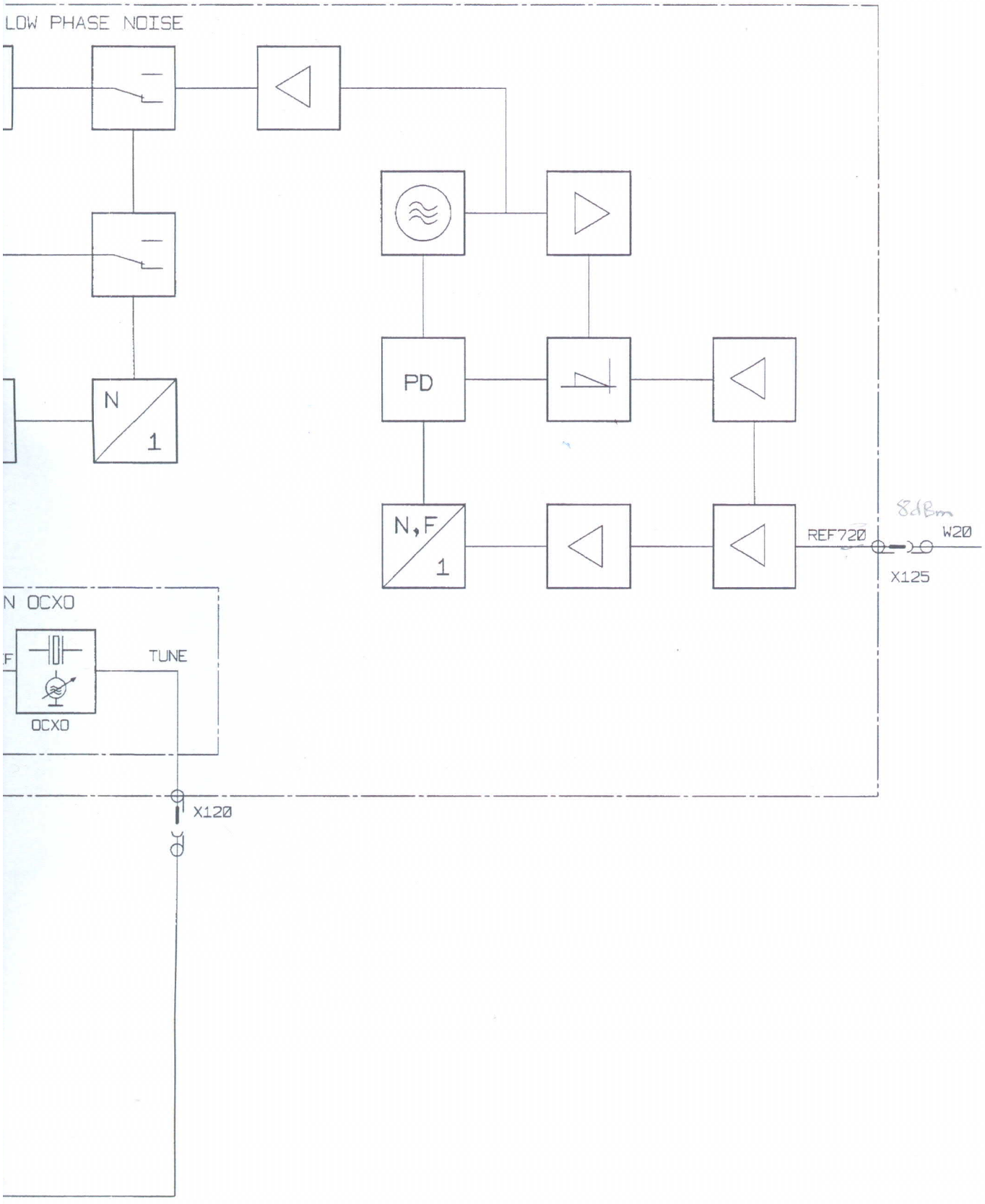
				GEPR.			
				NORM			
				PLOTT	26.04.95		top sheet3
				R/S ROHDE&SCHWARZ			ZEICHN.-NR. 1065.6000.01 S
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ZU GERAET FSEA			REG.I.V. 1065.6000 V ERSTE Z.

BLATT-NR. 4 v. 5 BL.


FRACSYN A140
BG-PORTS
X140
D A
TRANS PUTER
SWEEP LCA
FRAC SYN
N 1
W3
120M CAL OUT
X146
6 1
N 1
4/2 1
30/60 MHz
X147
EXT REF I/O
W14
N 1
VCXO
TCXO
D A
10 1
1MHz
PD
120 12 1
10MHz
OCXO-TUNE
X140


SAMPLE
W6
OPTION LOW PHASE NOISE
125 .. 700MHz
8dBm
X142
X123
W19
X122
PD
X145
20MHz TTL
0dBm
32 .. 90MHz
W18
X121
N
1
X141
PD
X143
W7
IFSYN
OPTION OCXO
10dBm
X128
10M REF
TUNE
OCXO
X149
W17
DC
YIGCON
REF 120M
X144
W8
120
12
1
X148
W21
ACHTUNG: EGB!
ELEKTROSTATISCH GEFAEHRDETE
BAUELEMENTE ERFORDERN EINE
BESONDERE HANDHABUNG.
ATTENTION ESD!
ELECTROSTATIC SENSITIVE DEVICES
REQUIRE A SPECIAL HANDLING
01/02
AEND.
IND.



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				GEPR.			
				NORM			
				PLOTT	26.04.95		top sheet4
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ROHDE&SCHWARZ			ZEICHN.-NR. 1065.6000.01 S
				ZU GERAET FSEA			REG.I.V. 1065.6000 V ERSTE Z.

BLATT-NR. 5 V. 5 BL.

ROHDE&SCHWARZ

SERVICE DOCUMENTS
Attenuator

1067.7755.02

Contents

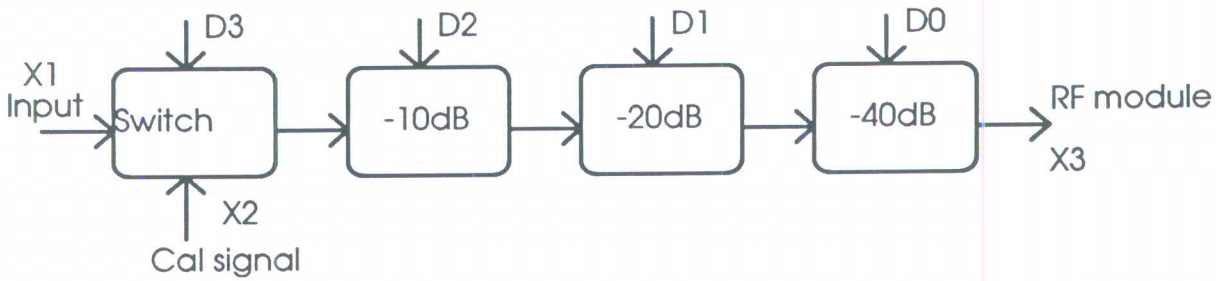
7 Testing the Module

7.1 Function Description

The module consists of three switchable attenuator pads (10 dB, 20 dB, 40 dB) and a switch used for switching the internal calibration generator to the RF input. The switches are bistable and are switched by a short pulse through a driving coil. Following the switchover, the current through the driving coil is switched off.

The control is effected by the level transputer via the serial bus. The board contains an EEpom as data storage for the frequency response correction, which is read when the instrument is started.

7.1.1 Block Diagram



7.2 Measuring Instruments and Auxiliary Equipment

Item	Type of instrument	Specifications	Appropriate R&S device	Order No.	Use
1	Digital multimeter	1 m V to 100 V 0.1 mA to 1 A	UDS5	349.1510.02	
3	Signal generator	100 kHz to 3500 MHz	SMHU	835.8011	
4	Spectrum analyzer	100 kHz to 1 GHz	FSA	804.8010.52	
5	Network analyzer	300 kHz to 7000 MHz			

7.3 Troubleshooting

7.3.1 Preliminary Remark

For all measurements, the level applied at sockets X1, X2 and X3 must not exceed the value 30 dBm = 1 W = 7 V into 50 Ω.

7.3.1.1 No Calibration Signal

When the service function *INPUT CAL* is activated, a signal with 120 MHz, -40 dBm must be measured.
If there is a level error, the attenuator should be set to an attenuation of 0 dB first
If there is no signal, check the signal at the calibration input of the attenuator using a spectrum analyzer:

Signal at X2 with activated service function *INPUT CAL*: 120 MHz, -40 dBm

If there is no such signal, the error is to be traced on the Fracsyn module.
If there is a calibration signal, the attenuation steps of the attenuator are checked:

Connect the pectrum analyzer to the attenuator output and measure signal level at 120MHz:
Set attenuator to 0 dB attenuation : level -40 dBm
Set attenuator to 10 dB attenuation : level -50 dBm
Set attenuator to 20 dB attenuation : level -60 dBm
Set attenuator to 40 dB attenuation : level -80 dBm

7.3.1.2 Level Error depending on Reference Level Set

First check whether the attenuator is switched:
Vary the attenuation manually from 0 dB to 70 dB in the *INPUT* menu using the Step keys. With each variation, a mechanical switching noise must be audible.
Apply a signal with 120 MHz, -20 dBm at the RF input of the FSE or switch in internal calibration signal using the service function *INPUT CAL*.

Connect the spectrum analyzer to the attenuator output (X3) and measure signal level at 120 MHz:
Set attenuator to 0 dB attenuation : level -40 dBm
Set attenuator to 10 dB attenuation : level -50 dBm
Set attenuator to 20 dB attenuation : level -60 dBm
Set attenuator to 40 dB attenuation: level -80 dBm

If there are all signals, the attenuator can be excluded as the error source.

7.4 Testing the Specifications

7.4.1 Testing the Attenuation Characteristic at RF

Connect the network analyzer to socket X1 and socket X3, set the attenuator to through-connection (0-dB position) and check the S21 parameters. Store the measured curve, in the following referred to as residual attenuation, in the network analyzer and subtract from the measured curve (reference value 0). Perform the next steps for each attenuator pad (Z1 to Z3) individually. Cut in attenuator pad, set the reference value on the analyzer according to the attenuation value. Check whether the tolerances indicated in the table are observed.

Attenuator steps	**10 dB**	**20 dB**	**40 dB**
max error for f <= 3.5GHz	0.25 dB	0.25 dB	0.5 dB
max error for 3.5 GHz < f <= 7G Hz	0.4 dB	0.4 dB	1.3 dB

Connect network analyzer to socket X1 and socket X3. Set the attenuator to through-connection and check the VSWR in the frequency range 50 MHz to 7 GHz. Repeat the measurement for each attenuator pad additionally cut in. Now actuate switch S to check whether connector X1 is terminated with 50 Ω . Connect network analyzer to X2 and X3 and repeat the procedure described above.

Frequency range	**Return loss**	**Residual attenuation X1 → X3**	**Residual attenuation X2 → X3**
f <= 1GHz	> 21 dB	< 0.8 dB	< 0.5 dB
1 GHz < f <= 3.5 GHz	> 13 dB	< 0.8 dB	
3.5 GHz < f <= 7 GHz	> 10 dB	< 0.8 dB	

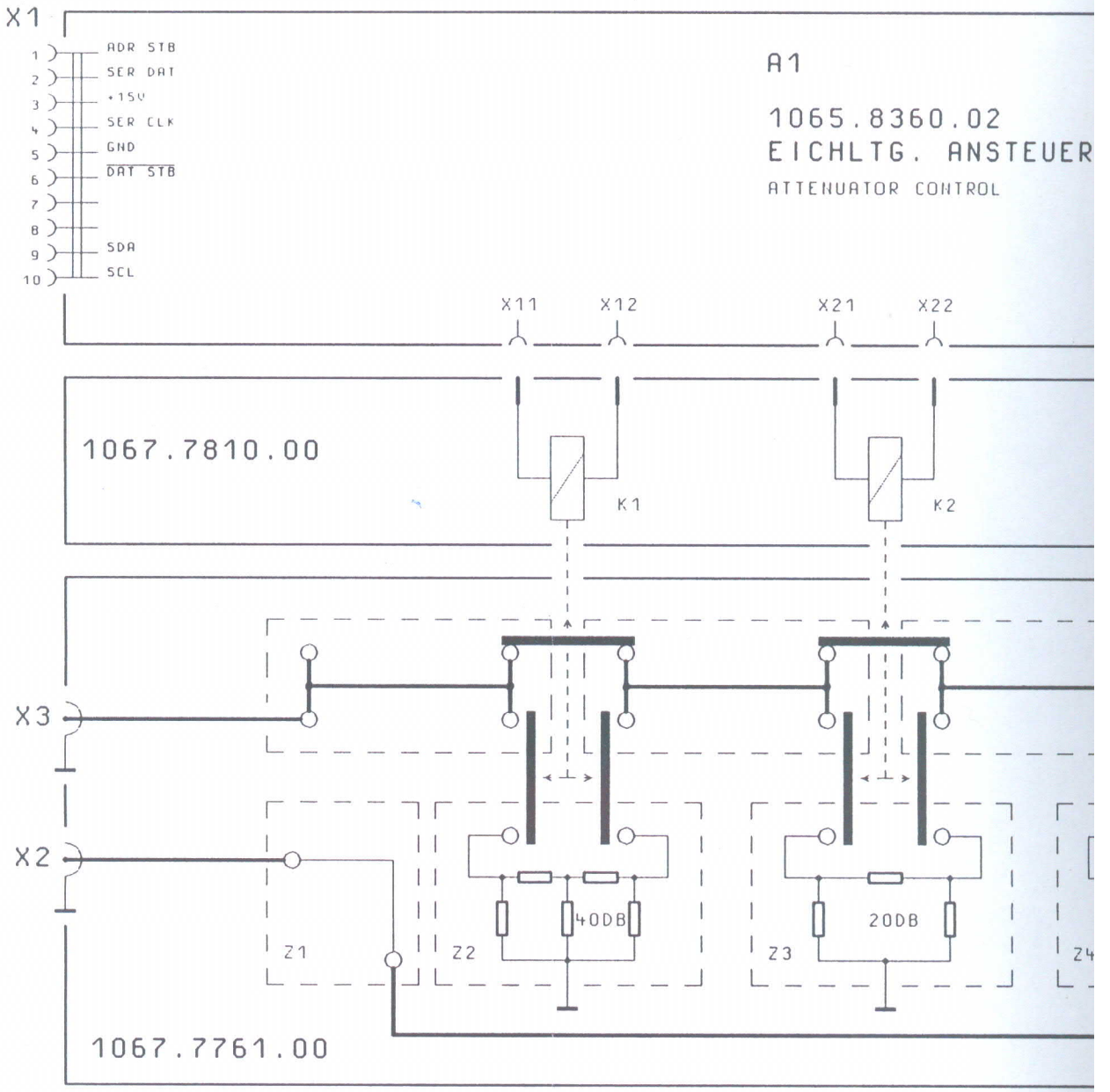
7.5 External Interfaces

Pin	Name	Input/ Output	Value range	Signal description
X101 1	PTP_STRA	E	TTL	Address strobe
X101 2	PTP_DAT	E	TTL	ser. data
X101 3	+15V__A			
X101 4	PTP_CLK	E	TTL	ser. clock
X101.5	GND_A			
X101 6	PTP_STRD	E	TTL	Data strobe
X101 9	PTP_SDA	B	TTL open collector	I²C-bus data
X101 10	PTP_SCL	E	TTL	I²C-bus clock
X1	RF input	E	0 to 7 GHz	
X2	Cal input	E	0 to 1 GHz	
X3	RF output	A	0 to 7 GHz	

ROHDE&SCHWARZ

Stromläufe
Bestückungspläne
Circuit diagrams
Components plans
Schémas de circuit
Plans des composants

(R 29500 Bl. 4)
095.1000 Bl. 4



DAEMPFUNGSGLIEDER EINGESCHALTET BEI
UEBERGANG VON HIGH NACH LOW

ATTENUATOR PADS SWITCHED ON HIGH SIGNAL
WITH TRANSITION FROM HIGH TO LOW

02

AENI
IND

)2
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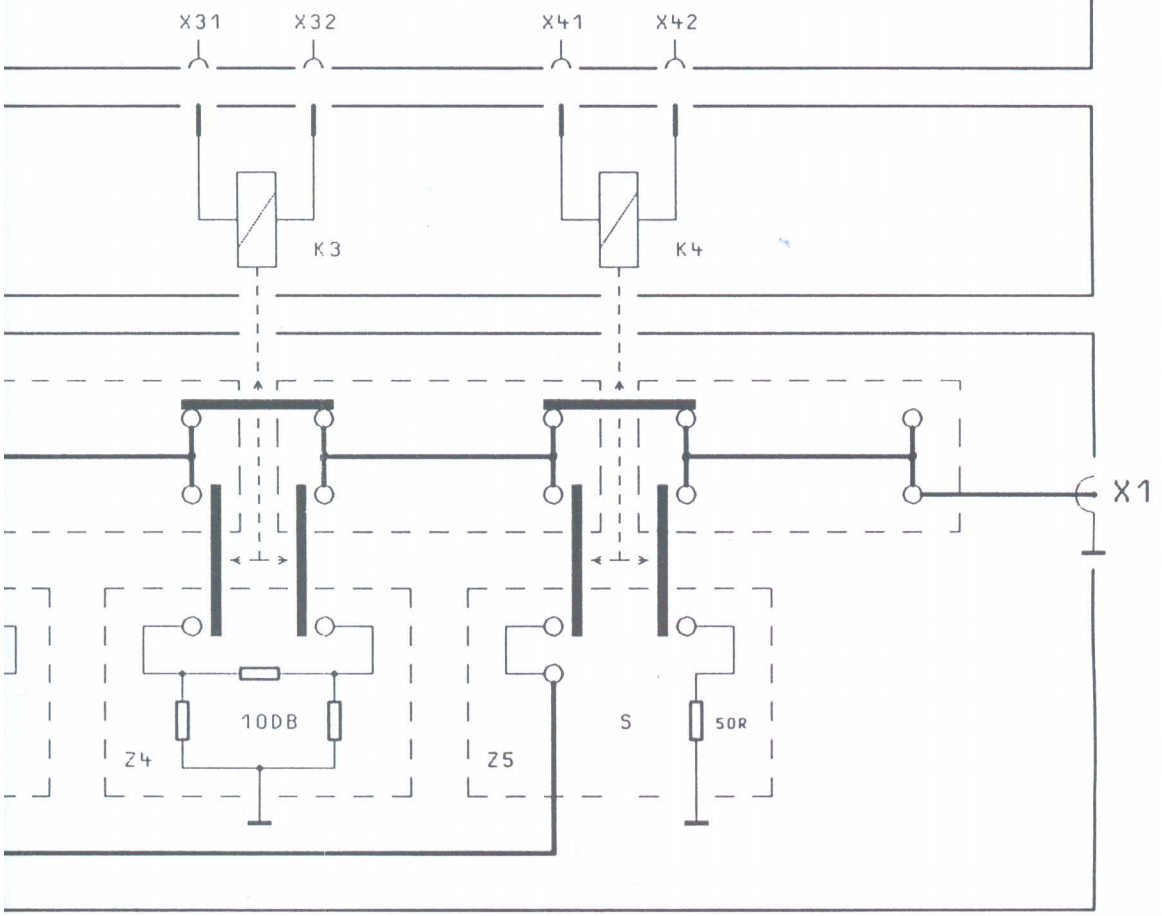


STROMLAUF GILT FUER VAR03 - SERIELLE ANSTEUERUNG

CIRCUIT DIAGRAM IS VALID FOR MOD03 - SERIAL CONNECTION

02				1CMK	TAG	NAME	BENENNUNG
				BEARB.	03.94	NG	ZE EICHLTG. 4-STUFIG FSE
				GEPR.			4-STEP ATTENUATOR FSE
				NORM			
				PLOTT			
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ROHDE&SCHWARZ			ZEICHN.-NR. 1067.7755.01S
				ZU GERAET FSE			REG.I.V. 1067.7490 ERSTE Z.

BLATT-NR. 1- V. BL.

ROHDE&SCHWARZ

SERVICE DOCUMENTS
RF MODULE

1065.6768.02

Contents

7 Testing the Module

7.1 Function Description

7.1.1 Function inside the Instrument

The RF MODULE converts the input signal of the analyzer from 0 to 3.5 (7) GHz to the first IF of 4341.4 (7941.4) MHz, and then to the second IF of 741.4 MHz.

7.1.1.1 Description of the Block Diagram

The RF MODULE is controlled by the frequency transputer.

The models of the FSE family are equipped with different RF MODULE versions:

- Mod. 02: input frequency range 0 to 3.5 GHz.
- Mod. 03: input frequency range 0 to 3.5 GHz, including the Option LO suppression and RF Overload Detector.
- Mod. 04: input frequency range 0 to 7 GHz.
- Mod. 05: input frequency range 0 to 7 GHz, including the Option LO suppression and RF Overload Detector.

The RF module consists of the motherboard and the modules YIG SAMPLER and RF CONVERTER.

YIG SAMPLER

The YIG SAMPLER module contains the YIG oscillator for generation of the 1st LO signal, a buffer and output amplifier as well as the sampling mixer. With the multiplied output signal of the FRAC SYN or LOW PHASE NOISE, the oscillator signal is converted to an IF of 5 to 100 MHz. This IF signal is used for synchronization of the YIG oscillator in the main loop.
The module for models 04 and 05 additionally includes a frequency doubler.

RF CONVERTER

The RF CONVERTER module contains the first mixer, the amplifier for the first LO, the first IF filter, the first IF amplifier and the second mixer. The input signal is converted to an IF of 741.4 MHz by way of two conversions.
The module for model 04 additionally includes a frequency doubler and an amplifier for the 2nd LO.
The module for models 03 and 05 additionally contains an overload detector at the first IF and a circuit for suppression of the first LO.

Motherboard

The two modules are mounted on the motherboard. It contains the interface to the frequency transputer, the bias setting for the two modules, driver circuits for the YIG tuning, a switchable voltage source for the noise source and the voltage regulator for supply of the antenna code socket.
The EEPROM on the motherboard contains correction data for the frequency response and the amplification of the RF CONVERTER module.

7.2 Measuring Instruments and Auxiliary Equipment

Item	Type of instrument	Specifications	Appropriate R&S device	Order No.	Use
1	Digital multimeter	1 mV to 100 V 0.1m A to 1 A	UDS5	349.1510.02	
2	Signal generator	100 kHz to 3500 (7000)MHz	SMHU (SMP)	835.8011	
3	Signal generator	100kHz to 3500 (7000)MHz	SMHU (SMP)	835.8011	
4	3-dB coupler	Decoupling >20dB; 1 to 3500 (7000) MHz			
5	Spectrum analyzer	100 kHz to 8000 MHz	FSM	1020.7020.52	
6	Power meter	100 kHz to 7000 MHz	URV5 NRV-Z2	349.8012.02	

7.3 Troubleshooting

Using the following description, an error on the RF MODULE can be clearly located. In the case of an error, the RF MODULE or one of the two modules is to be replaced.

Module replacement

- When replacing the motherboard or the YIG SAMPLER module, it is necessary to check the YIG adjustment according to section 7.4.2.
- When replacing the motherboard, the operating voltage is to be adjusted using R5 to the value required for the respective model before mounting the RF CONVERTER module!
- When replacing the RF CONVERTER module, the correction data associated with the module are to be stored in the EEPROM (section 7.4.4).
- If only the motherboard is replaced, the correction data for the RF CONVERTER are to be saved prior to the replacement. After the replacement, the data are copied back to the EEPROM (section 7.4.4).
- The automatic selftest must run without errors after module replacement.

7.3.1 Selftest

14 selftest voltages can be measured on the module. These voltages are measured in the automatic selftest with certain instrument setups and checked to determine whether they lie within a given tolerance.

Note: *Proper functioning of the modules FRAC SYN, DETECTOR and the digital is a prerequisite for running the automatic selftest of this module. The automatic testing of the complete instrument is always aborted after the tolerance has been exceeded for the first time in order to avoid irrelevant error message. For further fault location with the aid of externally applied signals, the test functions can be called up manually in the Board Test menu.*

The valid default for the RF MODULE as well as the default for the respective test function are set automatically. The selftest voltage measured and the permissible tolerance limits appear on the analyzer display.

Default setting:	Center:	120 MHz
	Span:	Zero
	RF Attenuation:	0 dB
	Cal. generator:	0 dBm

Table 7-1 Test functions:

Test function	Description	Setting	Error message:
0	Test 1 to 13 Module test	Test 1 to 13	
1	Operating voltage 1 of RF Converter	TP 2	Supply RF Converter
2	Operating voltage 2 of RF Converter	TP 12	Supply RF Converter
3	Bias of 1st LO amplifier, only for mod.02, 03	TP 5	Bias 1st LO Amp.
4	Bias of 1st LO amplifier, only for mod. 04, 05	TP 3	Bias 1st LO Amp.
5	Bias of 1st IF amplifier, amplifier 1	TP 6	Bias 1st IF Amp. 1
6	Bias of 1st IF amplifier, amplifier 2	TP 8	Bias 1st IF Amp. 2
7	Bias of 2nd LO amplifier, only for mod. 04, 05	TP 4	Bias 2nd LO Amp.
8	Bias of 2nd LO amplifier, only for mod. 04, 05	TP 13	Bias 2nd LO Amp.
9	Operating voltage of YIG oscillator	TP 7	Supply YIG Osc.
10	Bias of isolation amplifier	TP 9	Bias ISO Amp.
11	Bias of 1st LO amplifier.	TP 11	Bias 1st LO Amp.
12	Bias of amplifier for LO doubler, only for mod. 04, 05	TP 10	Bias 1st LO Doubler
13	Level after 1st mixer, only for mod. 03, 05	TP 0	IF Level
14	Temperature of RF Converter	TP 1	

Individual polling of the test signals without the associated instrument setup is also possible using a service function:

```
SERVICE FUNCTION
    2.11.1.X
```

`X = Number of test point`

7.3.2 Error in the Converter

Repair of the RF CONVERTER module is not possible. It is replaced in the case of an error. The supplied correction data are to be copied to the EEPROM of the module in this case (section 7.4.4).

7.3.2.1 Conversion Attenuation too large

An excessive attenuation can be caused by a fault in the RF CONVERTER itself or by a too small level of the first or second LO. Therefore, the output level of the YIG SAMPLER should be checked at socket X22 and the level of the 2nd LO at socket X151 of the 2nd IF CONVERTER. If the LO levels are okay, the error lies in the CONVERTER. By checking the biases according to section 7.4.3.1, it is possible to determine whether the fault lies in the CONVERTER or in the motherboard (test functions 1..5, 8, 9). If all biases are okay, the first mixer is probably faulty (see also 7.3.2.3). In this case check the conversion attenuation according to section 7.4.3.2.

7.3.2.2 Frequency Response Error

The frequency response of the RF CONVERTER is stored as correction data set in the EEPROM of the module and is corrected by a calibration amplifier on the IF Filter module (CAL AMP1) in the measurement. If a frequency response error occurs although the calibration amplifier functions properly (→ IF FILTER section 7.4.1), there is a fault in the RF CONVERTER or the EEPROM cannot be read.

7.3.2.3 Excessive LO Feedthrough

An excessive LO feedthrough indicates a faulty mixer; in the case of mod. 03, 05 the fault may also lie in the circuit for LO suppression. → Check the conversion attenuation and the frequency response and LO compensation.
Further hints at a faulty mixer are provided by a measurement of the forward voltage of the mixer diodes at the RF input:

- Set attenuator of FSE to 0 dB.
- Switch off instrument.
- Measure forward voltage of diodes at RF input in both directions. Nom. value: 900 mV ± 100 mV

7.3.2.4 Excessive Noise Display

In the case of an excessive noise display, check whether it is caused by the RF MODULE or the subsequent modules (→ 2nd IF CONVERTER, IF FILTER).

7.3.2.5 Too Small Intermodulation Ratio (IP3)

Check the intermodulation ratio according to section 7.4.3.3 at the frequency at which the error ocurs. If the fault lies in the RF MODULE, the LO levels are checked at output X22 of the YIG SAMPLER, or at output X151 of the 2nd IF CONVERTER. If these are okay, there is a fault in the RF CONVERTER.

7.3.2.6 Error in the RF Overload Display (Mod. 03, 05)

No RF overload display although mixer level > + 10 dBm

Overload detector on RF MODULE faulty. Check according to 7.4.3.6.

Permanent RF overload display even without signal

- Remove RF cable from input X152. If the RF overload display disappears, it is caused by the 2nd IF CONVERTER. Further troubleshooting according to section 7 of the 2nd IF CONVERTER.
- If the RF MODULE still causes an overload, the detector on the module is faulty.

7.3.3 Error in the YIG SAMPLER

If an error is assumed to lie in the YIG SAMPLER, check the biases according to section 7.4.2.1.

7.3.3.1 LO Level

If the LO level is too small, no signal or a signal with large level error is visible on the display. Another resulting error may be a poor intermodulation ratio. In these cases, the LO level should be checked directly at output X22 of the YIG SAMPLER. If the following error messages occur during the selftest, there may also be a fault in the LO section of the YIG SAMPLER:

- Error with test function 10, 11, 12:	Error in YIG SAMPLER
- Error with test function 9:	Supply voltage of YIG oscillator faulty. → Check motherboard.

7.3.3.2 Error in the Coarse Tuning (Main Coil)

The control voltage for the coarse tuning is generated by the FRAC SYN module. If the measured values at X130.C15 are out of tolerance, open the connection at the service adapter to determine whether there is a fault in the FRAC SYN module or in the motherboard.

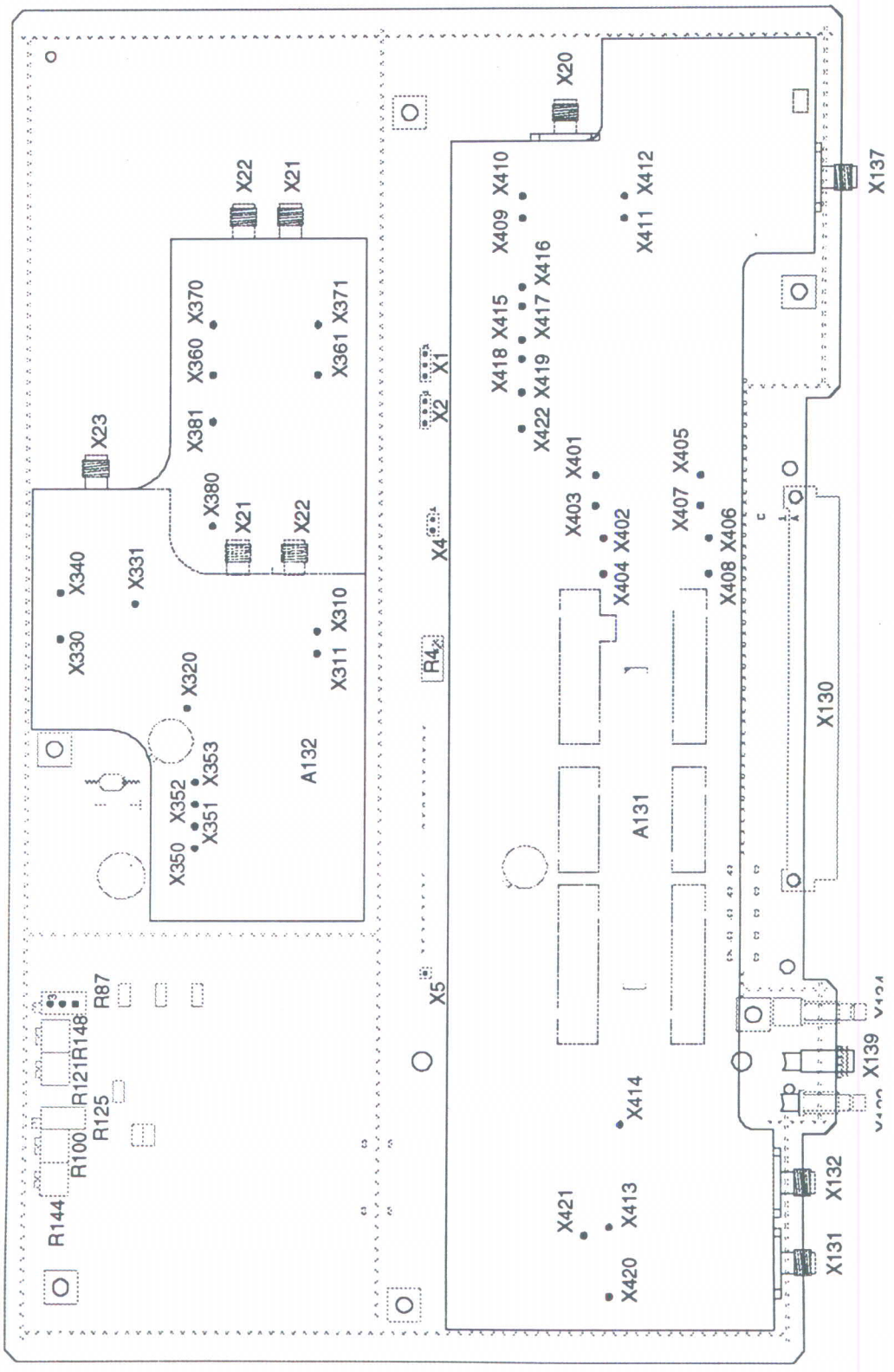
- Tuning voltage okay:	Check coarse tuning according to section 7.4.2.2. If necessary, perform YIG adjustment.
- Tuning voltage still faulty after opening the connection:	Error in FRAC SYN or short-circuit on the motherboard
- Tuning voltage okay after opening the connection:	Main coil driver faulty (motherboard).

7.3.3.3 Error in the Fine Tuning (FM Coil)

In the case of an error in the fine tuning, the YIG oscillator can no longer be synchronized (error message LO unlock, voltage YIGCON out of tolerance). This may also be caused by faulty adjustment of the coarse tuning, a faulty dynamic YIG adjustment or an error in the YIG control loop (→ FRAC SYN). If the adjustments mentioned cannot be performed, check the fine tuning according to section 7.4.2.3.

7.4 Testing the Specifications

7.4.1 Position of Jumpers, Test Points and Adjustment Devices



7.4.2 First LO

Proper functioning of the FRAC SYN module is a prerequisite for performing the following tests.

7.4.2.1 Biases

Operate the module outside the instrument using the FSE service kit.

Test point	Mod.02, 03	Mod. 04, 05	Remark:
X310	-	+ 6.5 V ± 0.1 V	RF MODULE TF 10
X311	-	0 to - 2 V	
X320	+ 12 V	+ 12 V ± 0.1 V	
X330	+ 12 V	+ 12 V ± 0.1 V	
X340	+ 14.2 V	+ 14.2 V ± 0.1 V	
X352	- 5 V	- 5 V ± 0.1 V	RF MODULE TF 9
X353	+ 15 V	+ 15 V ± 0.1 V	
X360	+ 6.5 V	+ 6.5 V ± 0.1 V	RF MODULE TF 12
X361	0 to - 2 V	0 to - 2 V	
X370	-	+ 7.0 V ± 0.1 V	RF MODULE TF 11
X371	-	0 to - 2 V	
X380	-		
X381	-		

7.4.2.2 Coarse Tuning

Test setup:

- Connect spectrum analyzer to X22.
- Remove cable from X139.

Measurement:

Setting on the FSE: SPAN Zero

- Measure YIG frequency and tuning voltage at the following frequencies:

CENTER frequency on FSE	Voltage between X130.C15 and X130.C16	YIG frequency at X22	Voltage at R87, Pin 3
0 Hz	FSEA: 1.4 V FSEB: 0.5 V	FSEA: 4341.4 MHz ± 20 MHz FSEB: 7941.4 MHz ± 40 MHz	FSEA: 1.6 V to 2.55 V FSEB: 1.5 V to 2.35 V
FSEA: 3.5 GHz FSEB: 7 GHz	FSEA: 9.6 V FSEB: 8.8 V	FSEA: 7841.4 MHz ± 20 MHz FSEB: 14941.4 MHz ± 40 MHz	FSEA: 3.0 V to 4.7 V FSEB: 2.9 V to 4.4 V

The voltages at R87 vary with the static YIG adjustment.

7.4.2.3 Fine Tuning

Test setup:

- Connect spectrum analyzer to X22.
- Remove cable from X139.
- Connect voltage source to X139.

Measurement:

Setting on the FSE:

SPAN Zero
CENTER 0 Hz

- Set voltage at X139 to 0 V.
- Measure frequency at X22. FSEA: 4341.4 MHz ± 20 MHz
  FSEB: 7941.4 MHz ± 40 MHz
- Set voltage at X139 to - 8 V.
- The frequency at X22 varies by FSEA: - 40 MHz
  FSEB: - 80 MHz
- Set voltage at X139 to + 8 V.
- The frequency at X22 varies by FSEA: + 40 MHz
  FSEB: + 80 MHz

7.4.2.4 LO Output Level

Test setup:

- Connect spectrum analyzer to X21, or X22.
- Remove cable from X139.

Measurement:

Setting on the FSE:

SPAN Zero

- Vary center frequency between 0 Hz and 3.5 (7) GHz
- Measure LO level:

FSEA, X22: > +14 dBm in the frequency range 4.34 to 7.84 GHz

X21: > -18 dBm

FSEB, X22: > +12 dBm in the frequency range 7.94 to 14.94 GHz

X21: > 0 dBm in the frequency range 7.5 to 15.2 GHz

7.4.2.5 IF Level

Test setup:

- Connect spectrum analyzer to X134.
- Remove cable from X139.

Measurement:

Setting on the FSE:

SPAN Zero

- Vary center frequency between 0 Hz and 3.5 (7) GHz
- Measure IF level at X134.

Frequency: 30 MHz ± 20 MHz

Level: - 18 dBm ± 4 dB

Umbau YIG – Abgleich

After execution of the modifications and programming of the new firmware the synchronisation can be adjusted. If the 0 Hz carrier is jumping you should execute the following adjustment:

PRESET . R125: 0 MHz Linie auf 0 MHz abgleichen
activate the service function. The password is 894129. MHz
Enter service function 2.10.1.13

FREQUENCY CENTER 1 MHZ, SPAN 0 MHZ

The selftest voltage will appear in the lower left corner. It should be 0 V, +- 0.2 Volt. It can be adjusted with R125 on the RF-Module (accessible from the top).

FREQUENCY CENTER 3.49 GHZ, SPAN 0 MHZ

The selftest voltage will appear in the lower left corner. It should be 0 V, +- 0.2 Volt. It can be adjusted with R87 on the RF-Module (accessible from the top).

Check at 1 MHz again to compensate influence of R87.
Enter 2.10.0 to deactivate the service function
After this static adjustment the dynamic synchronisation should be done:
(die [illegible] anzeige [illegible] am Bildschirm)

PRESET

Connect a scope to the testpoint.

If you have a DEMO-FSEA the testpoint is located on the RF-Unit, componenet side. In the upper left corner, you should see 2 pairs of PCB-pads. Touch the upper right one with the probe tip.

If your FSEA is newer and not a demo, connect the scope to the motherboard, X130 (Rf-module socket) pin A17.

You will see the FM coil correcting voltage during the full span sweep. During the valid period this signal must not exceed +- 4 Volts. The valid period starts from sweep start and is 3 ms long, then follows a burst packes which will exceed the tolerance, then another valid period of 4 ms length. The correct voltage can be adjusted with R 121 and R148. Normaly the adjustment will be near CCW position.
DO NOT ADJUST BOTH POTS TO CCW! (self oscillation).

If you have question you can contact 3MSF +49-89-4129-2576

7.4.2.6 Static YIG Adjustment

Test setup:

- Connect spectrum analyzer to X21.
- Reconnect cable from X139 to X148.
- Connect multimeter to X130.A17 (test output YIGCON).

Measurement and adjustment:

Setting on the FSE:

SPAN	Zero
CENTER	0 Hz

- Set R125 such that the YIG oscillator locks in at 4341.4 (7941.4) MHz and the voltage at X130.A17 reads 0 V ± 100 mV.
- Set center frequency to 3.5 (7) GHz.
- Set R87 such that the YIG oscillator locks in at 7841.4 (14941.4) MHz and the voltage at X130.A17 reads 0 V ± 100 mV.
- Repeat adjustment steps at center frequency 0 Hz and 3.5 (7) GHz until the voltage at X130.A17 is equal to 0 V ± 100 mV at both frequencies.

7.4.2.7 Dynamic YIG Adjustment

Test setup:

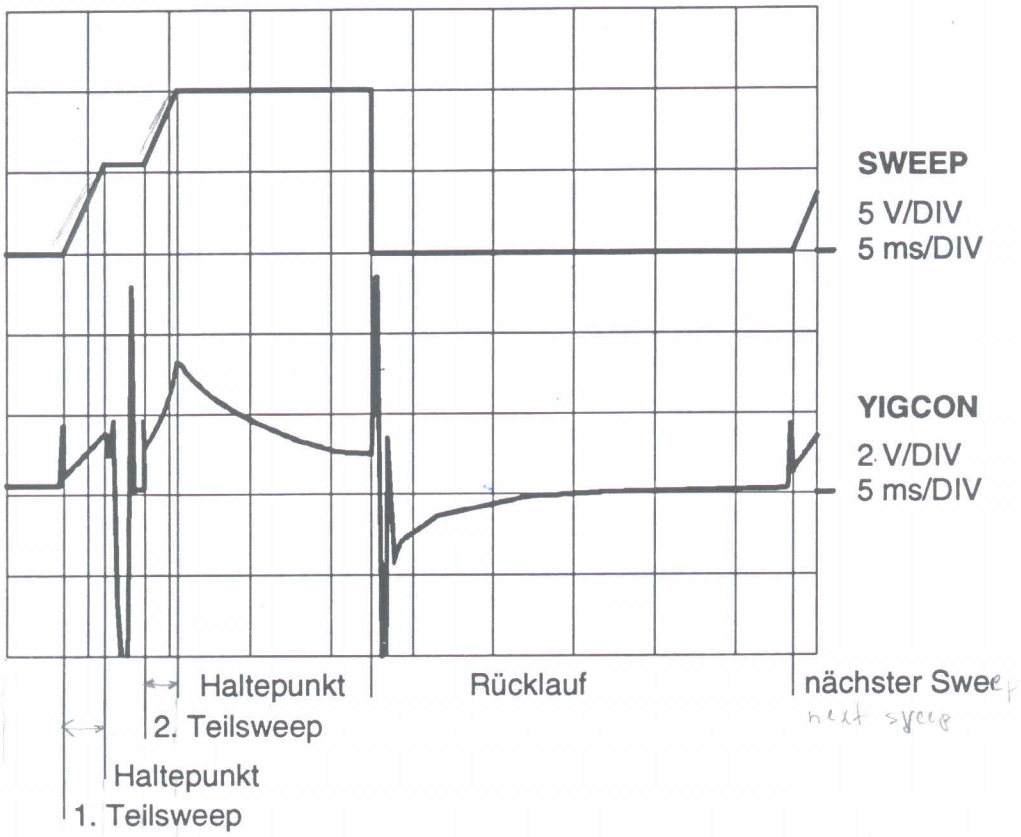
- Connect oscilloscope channel 1 to SWEEP socket (trigger signal).
- Connect oscilloscope channel 2 to X130.A17 (test output YIGCON).

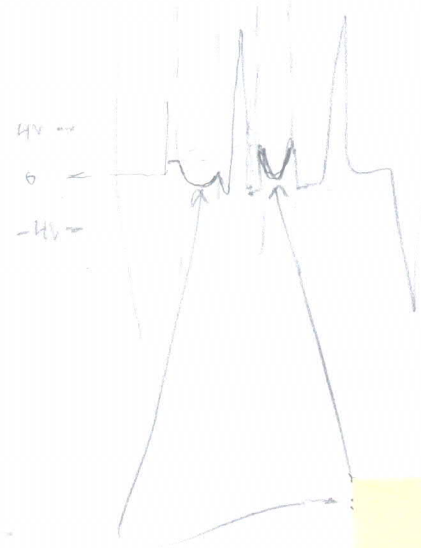
Measurement and adjustment:

Setting on the FSE:

SPAN	Full
SWEEPTIME	5 ms

- Set R148 and R121 such that the voltage at X130.A17 does not exceed a value of ± 4 V during the two sweeps.


SWEEP
5 V/DIV
5 ms/DIV
YIGCON
2 V/DIV
5 ms/DIV
Haltepunkt
2. Teilsweep
Haltepunkt
1. Teilsweep
Rücklauf
nächster Swee
next sycc



7.4.3 RF CONVERTER

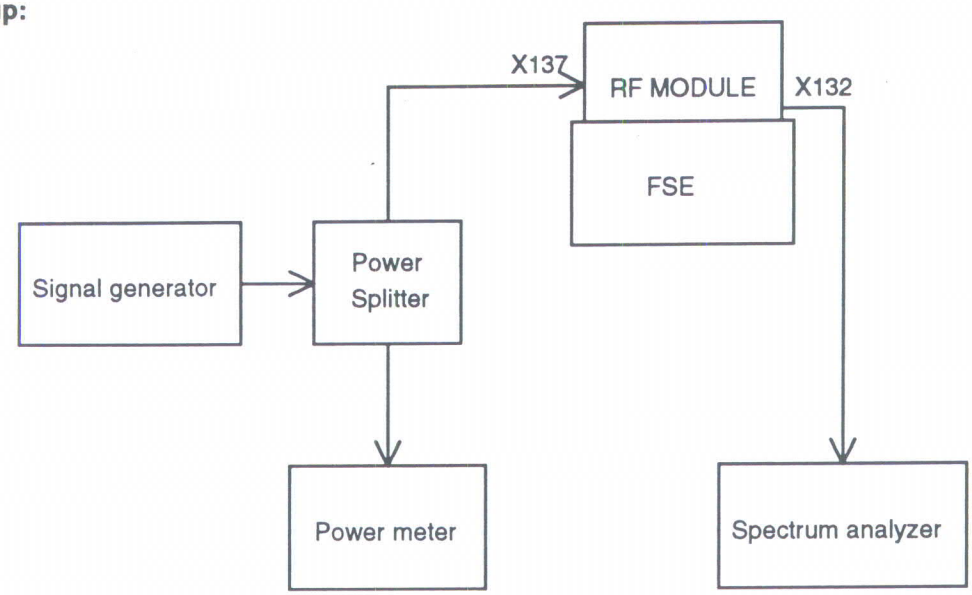
7.4.3.1 Biases

Test point:	Mod. 02, 03	Mod. 04, 05	Remark:
X5	7.0 V ± 50 mV, 6.5 V ± 50 mV, after board version -04-	7.5 V ± 50 mV	Use R4 to adjust to nominal value. RF MODULE TF 1
X403, X404	+ 4.0 V ± 0.1 V	+ 4.0 V ± 0.1 V	RF MODULE TF 6
X401, X402	0 to - 1 V	0 to- 1 V	
X407, X408	+ 4.0 V ± 0.1 V	+ 4.0 V ± 0.1 V	RF MODULE TF 5
X405, X406	0 to - 1 V	0 to - 1 V	
X411	-	+ 7.0 V ± 0.1 V	RF MODULE TF 4
X409	-	- 0.1 to - 1.5 V	
X412	+ 6.0 V ± 0.1 V	-	RF MODULE TF 3
X410	- 0.1 to - 1.5 V	-	
X420	-	+ 5.2 V ± 0.1 V	RF MODULE TF 7
X421	-	+ 5.2 V ± 0.1 V	RF MODULE TF 7
X414	-	+ 7.0 V ± 0.1 V	RF MODULE TF 8
X413	-	- 0.1 to - 1.5 V	

7.4.3.2 Conversion Attenuation

The attenuation and the frequency response of the module are stored in the EEPROM. Recalibration of the module is only possible using a special test station. The following test is used to check whether the conversion attenuation lies within the permissible tolerance.

Test setup:



Measurement:

Setting on the FSE:

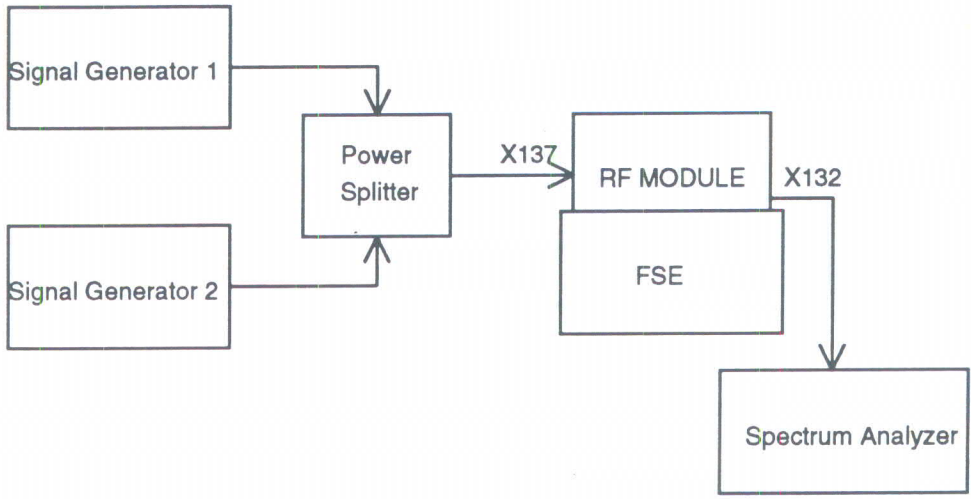
SPAN Zero

- Calibrate level display of spectrum analyzer at 741.4 MHz.
- Set center frequency to transmitter frequency.
- Set transmitter level to -5 dBm using power meter.
- Determine conversion attenuation for frequencies 10 to 3500 MHz (7000 MHz):

Frequency range	Mod. 02, 03	Mod. 04, 05
10 to 3500 MHz	7.5 dB to 11.5 dB	-
10 to 6500 MHz	-	9 dB to 15 dB
6500 to 7000 MHz	-	12 dB to 18 dB

7.4.3.3 Intermodulation (IP 3)

Test setup:



Measurement:

Setting on the FSE:

SPAN	Zero
CENTER	respective test frequency

- Set transmitter 1 to center frequency.
- Set transmitter 2 to center frequency + 1 MHz.
- Set the level of the individual signals to -10 dBm.
- Measure level at X132 at 741.4 MHz (= reference value).
- Set transmitter 1 to center frequency + 2 MHz.
- Measure level at X132 at 741.4 MHz.

  Difference from reference value: > 50 dB

- Repeat measurement for different center frequencies.

7.4.3.4 LO Feedthrough

Test setup:

- Terminate RF input with 50 Ω.
- In the case of mod. 03, 05 call the function LO Sup. in the CAL menu.

Measurement:

Setting on the FSE:	SPAN	Zero
	CENTER	0 Hz
	RF Attenuation	0 dB

Mod. 02, 04:

- Read LO level on the display. Nom. value: < - 8 dBm

Mod. 03, 05:

- Read LO level on the display. Nom. value: < - 45 dBm

7.4.3.5 Overload Detector (Mod. 03, 05)

Test setup:

- Connect signal generator to RF input.
- Terminate output of RF MODULE with 50 Ω.

Measurement:

Setting on the FSE:	CENTER	120 MHz
	SWEEP	Single Sweep

- By starting the sweep an interrupt reset is triggered.

Signal generator: 120 MHz Level	**Action**	**Logic level at X140.C20**
0 dBm	Interrupt Reset	High
+ 10 dBm	Interrupt Reset	Low

7.4.4 EEPROM Data

Using a service function, the complete EEPROM contents can be read out to the hard disk of the instrument and written back.

SERVICE FUNCTION 2.11.3.X	X=0: Read out EEPROM data. X=1: Write back EEPROM data.

The directory D:\RUNTIME\CAL\ then contains the file RF.DAT. When replacing an individual module or the motherboard, the file must be updated. For further information refer to the supplement to the replacement module.

7.5 External Interfaces

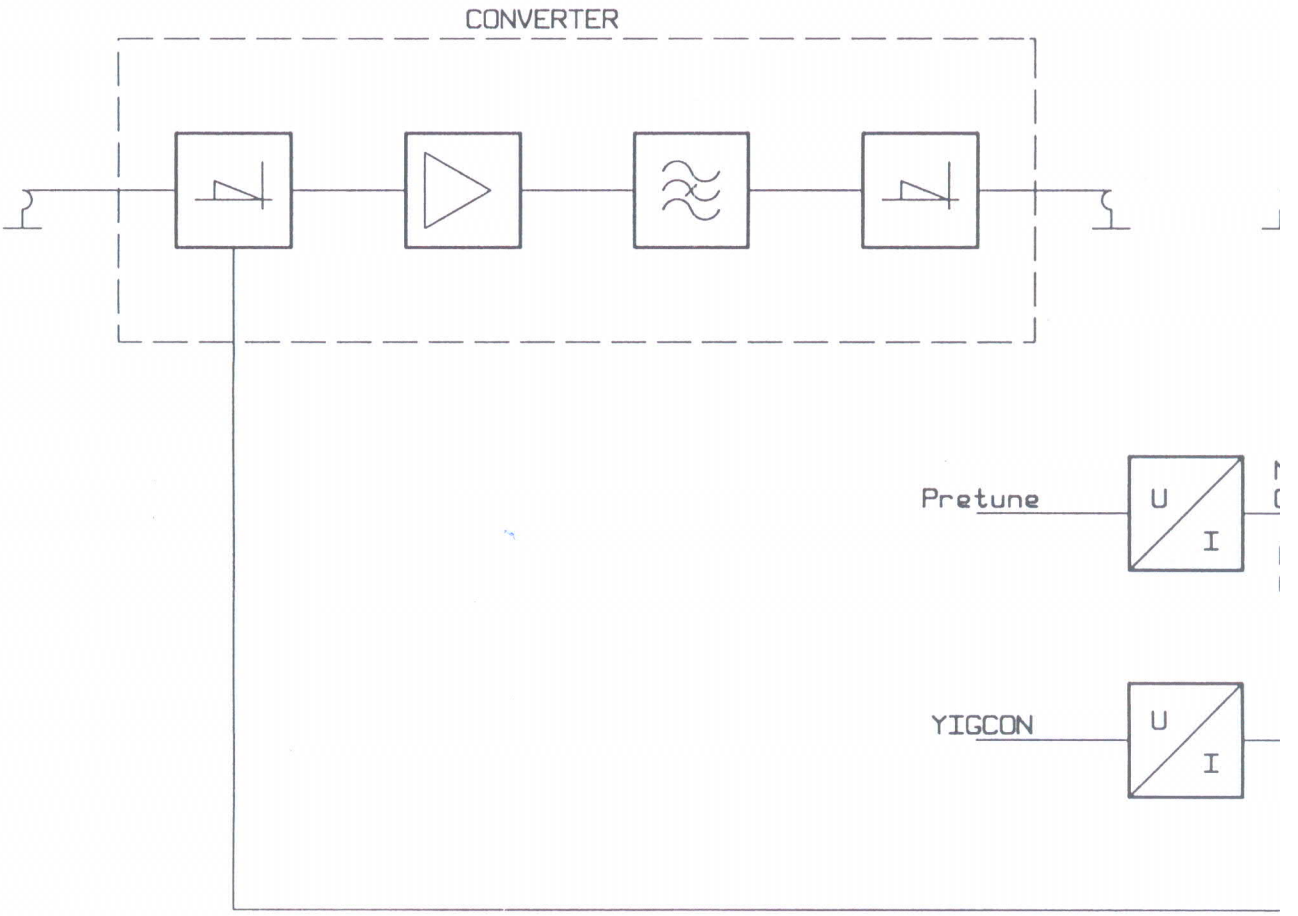
Pin	Name	Input/ Output	Origin/Destination	Value range	Signal description
A1	nREADY	E	FRAC SYN	TTL	Data ready
C1	TEMPFE	A	POWER SUPPLY	3 +- 0.25 V	Temperature sensor
C2	TEMPFE-GND	A	POWER SUPPLY	0 +- 10 mV	Temperature sensor GND
A10	FTP_CLK	A		TTL	Interface to frequency transputer, clock
C10	FTP_DAT	A		TTL	Interface to frequency transputer, data
A11	FTP_STRA	A		TTL	Interface to frequency transputer, address strobe
C12	FTP_STRD	E		TTL	Interface to frequency transputer, data strobe
C15	PRETUNE	E	FRAC SYN	0 to 10 V	YIG coarse tuning
C16	GNDDAC	E	FRAC SYN	0 V ± 10 mV	Reference for tuning volt.
A17	YIGCON	E	FRAC SYN	- 15 V to + 15 V	YIG fine tuning, test output
C21	RF_OVR-10	A	DETECTOR	open Collector	Overload detector
C20	RF_OVR	A	DETECTOR	open Collector	Overload detector
A24	INTRES	E	DETECTOR	TTL	Reset error message
A25	ADCMUX	A		-5V to +5V	Test channel for selftest
A26	ADCGND	B		0V	Reference ADCMUX
C26	F_SDA	E		TTL, 100 kHz	I^2C bus
C27	F_SCL	E		TTL, 100 kHz	I^2C bus
C28	+28V	E		+28 V ± 1 V	Supply
A29	-15V	E		-15 V ± 0.1V	Supply
B29	-15V	E		-15 V ± 0.1 V	Supply
C29	-15V	E		-15 V ± 0.1 V	Supply
A30	+15V	E		+15V ± 0.1 V	Supply

Pin	Name	Input/ Output	Origin/destination	Value range	Signal description
B30	+15V	E		+15 V ± 0.1 V	Supply
C30	+15V	E		+15V ± 0.1 V	Supply
A31	+5V_A	E		+5.5 V ± 0.05V	Supply
B31	+5V_A	E		+5.5 V ± 0.05 V	Supply
C31	+5V_A	E		+5.5V ± 0.05 V	Supply
A32	GNDA	B		0 V	Ground analog
B32	GNDA	B		0 V	Ground analog
C32	GNDA	B		0 V	Ground analog
X131	RF_IN	E		Mod. 02, 03: 0 to 3.5 GHz, max. - 10 dBm Mod. 04, 05: 0 to 7 GHz, max. - 10 dBm	RF input
X132	2nd_LO	E	2ND IF CONVERTER	3600 MHz , > 18 dBm	2nd LO
X133	FRACSYN	E	FRAC SYN, LOW PHASE NOISE	485 MHz to 700 MHz, +10 to 14 dBm	Synthesizer signal
X134	IFSYN	A	FRAC SYN	< 100 MHz, - 15 dBm typ.	IF from YIG and comb signal
X135	1st LO	A		3.75-8 GHz - 10 dBm typ.	1st LO for tracking, socket optional
X137	2nf IF_OUT	A	2ND IF CONVERTER	741.4MHz Mixer level - 8 dB	IF output
X139	YIGCON	E	FRAC SYN	- 15 V to + 15 V	YIG fine tuning

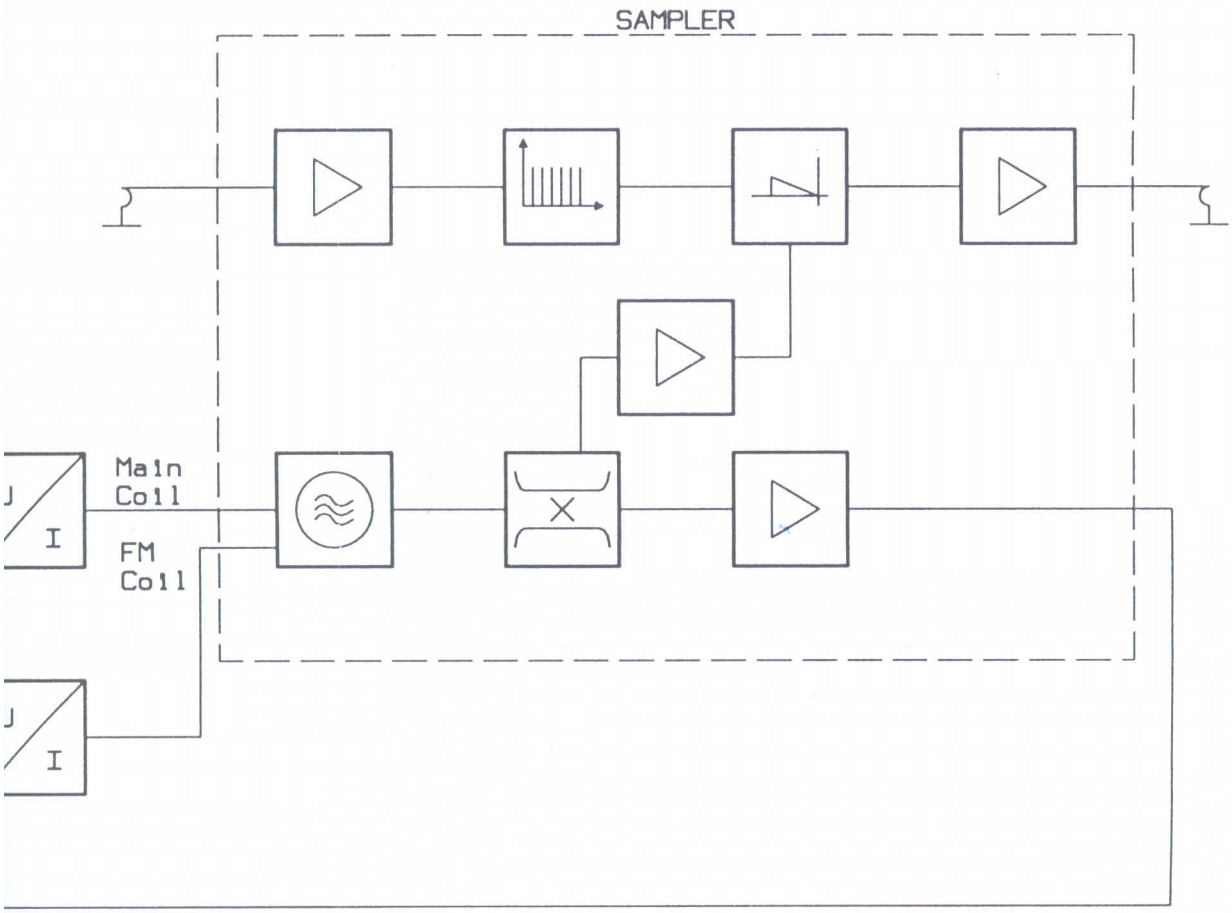
ROHDE&SCHWARZ

Stromläufe
Bestückungspläne
Circuit diagrams
Components plans
Schémas de circuit
Plans des composants

(R 29500 Bl 4)
095.1000 Bl. 4



ACHTUNG: EGB!
ELEKTROSTATISCH GEFAEHRDETE
BAUELEMENTE ERFORDERN EINE
BESONDERE HANDHABUNG.
ATTENTION ESD!
ELECTROSTATIC SENSITIVE DEVICES
REQUIRE A SPECIAL HANDLING



07				1ESK	TAG	NAME	BENENNUNG
				BEARB.		PF	RF_MODULE
				GEPR.		PF	RF_MODULE
				NORM			
				PLOTT	24.07.95		top sheet1
				ROHDE&SCHWARZ			ZEICHN.-NR. 1065.6774.01S BLATT-NR. 2
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ZU GERAET FSEA			REG.I.V. 1065.6000 ERSTE Z. 1065.6768 V.7 BL.

ROHDE&SCHWARZ

SERVICE DOCUMENTS
FRAC SYN

1065.7512.02

Contents

7 Testing the Module

7.1 Function Description

7.1.1 Function Inside the Instrument

The FRAC SYN module contains the reference frequency conditioning for the instrument, the frequency transputer for controlling all frequency-dependent module settings, a calibration signal source for instrument calibration, the sweep synthesizer and a phase-locked loop for the YIG synchronization.

7.1.1.1 Description of the Block Diagram

Reference frequency conditioning

A crystal oscillator supplies the 120-MHz reference signal. By means of frequency dividers, the frequencies 60, 30, 20 and 10 MHz are generated, which are used on the module itself or in the instrument.
The 120-MHz crystal oscillator is synchronized to a frequency-stable reference oscillator (a TCXO or OCXO with Option FSE-B4). With the external reference set, the 120-MHz oscillator can be synchronized to frequencies of 1 to 16 MHz (in 1-MHz steps) using a programmable divider. With internal reference, the module provides a 10-MHz signal at the rear-panel socket.

Frequency transputer (FTP)

The transputer on the FRAC SYN module, in the following referred to as frequency transputer, receives the current sweep setting via the level transputer from the graphics transputer. The frequency transputer thus calculates the required synthesizer settings. The settings required during the sweep are performed via a parallel bus. In addition to the control of the sweep synthesizer, several D/A converters are programmed in parallel during the sweep. These converters provide control voltages for a frequency-dependent level correction, the coarse tuning of the YIG oscillator and the control of the sweep output. For options like tracking generator and preselector, further D/A converters are provided on the module.
For control of the settings where timing is not critical, a serial bus is available to the frequency transputer.

Calibration signal source

Using a level control, the 120-MHz signal is adjusted to a constant level. Via switchable attenuator pads, a calibration signal with 0 or -40 dBm is provided.

Sweep synthesizer

The sweep synthesizer provides a signal between 475 MHz and 700 MHz, which can be set with a very small step size (< 0.1 mHz). This frequency resolution is achieved by a synthesizer operating according to the fractional N method. A VCO is synchronized to the 20-MHz reference via a programmable divider by means of a PLL. By switching between different division factors, an average division factor is obtained, which corresponds to a fractional division factor. The divider is controlled by a gate array, which is to be programmed only if the frequency is readjusted.

YIG control loop

A correction signal for the YIG fine tuning is derived from the IF signal of the YIG sampler and the internal 30 or 60-MHz reference signal. To this end, the module contains a phase detector and a control amplifier with loop filter with switchable control amplification. During operation with the LOW PHASE NOISE Option, the signal of the sweep syntheszier divided by 16 is used as reference. The respective divider is accommodated on the LOW PHASE NOISE module.

7.2 Measuring Instruments and Auxiliary Equipment

Item	Type of instrument	Specifications	Appropriate R&S device	Order No.	Use
1	Digital multimeter	1m V to 100 V 0.1 mA to 1 A	UDS5	349.1510.02	
2	Frequency counter	Accuracy $>1*10^{-8}$			
3	Signal generator	100 kHz to 3500 MHz	SMHU	835.8011	
4	Spectrum analyzer	100 kHz to 1000 MHz	FSA		
5	Power meter	100 kHz to 3500 MHz	URV5 NRV-Z5	349.8012.02	
6	Oscilloscope	100 MHz, 10:1 probe	BOS		

7.3 Troubleshooting

Using the following description, an error in the FRAC SYN module can be clearly located. In the case of an error, the module is to be replaced.

Module replacement

- When replacing the module, check the accuracy of the internal reference frequency and the level of the calibration signal source. If necessary, perform an adjustment in the instrument according to section 7.4.
- The automatic selftest must be run without errors after module replacement.

7.3.1 Selftest

14 selftest voltages can be measured on the module. These voltages are measured in the automatic selftest with certain settings and checked to determine whether they lie inside a given tolerance window.

Note: *Proper functioning of the frequency transputer, the DETECTOR module and the digital section is a prerequisite for funning the automatic selftest of this module. The automatic testing of the complete instrument is always aborted after the tolerance has been exceeded for the first time in order to avoid irrelevant error messages. For futher fault location also with the aid of externally applied signals, the test functions can be called up manually in the Board Test menu.*

The valid default for the FRAC SYN module and the default for the respective test function are set automatically. The selftest voltage measured and the permissible tolerance limits appear on the analyzer display.

Default setting: Center: 0 Hz

Span: Zero

Table 7-1 Test functions:

Test-function	Description	Setting	Error message:
0	Test 1 to 19 Module test. Test 1..3 depending on operating mode	Test 1 to 19	
1	Reference test	TP 6, TCXO-Betrieb	TCXO Level
2	OCXO test, if OCXO provided.	TP 9, OCXO operation	OCXO Level
3	External reference	TP 6 ext. Ref.	Ext. Ref. Level
4	120-MHz-VCXO test	TP 2	Level 120 MHz

Test function	Description	Setting	Error message:
5	Reference divider test	TP 5	Level Ref 20 MHz
6	120-MHz PLL	TP 2	Tuning Volt. VCXO
7	Reference output	TP 7	REF Output
8	VCO test, low frequency	TP 11, Center: 0 Hz	VCO Level
9	VCO tuning voltage low frequency	TP 10, Center: 0 Hz	Tuning Volt. VCO
10	VCO test, high frequency	TP 11, Center: 1798 MHz (FSEA) 2558 MHz (FSEB)	VCO Level
11	VCO tuning voltage high frequency	TP 10, Center: 1798 MHz (FSEA) 2558 MHz (FSEB)	Tuning Volt. VCO
12	Reference test, YIG loop	TP 4, cut in 30-MHz reference.	Level Ref. 30 MHz
13	IF level, f = 30 MHz	TP 12, 30-MHz-Ref.	IF Level
14	YIG tuning voltage, low frequency	TP 13, 30-MHz-Ref.	Tuning Voltage YIG
15	Reference test, YIG loop	TP 4, 60-MHz reference	Level Ref. 60 MHz
16	IF level, f = 60 MHz	TP 12, 60-MHz ref. Center: 0 Hz	IF Level
17	IF level	TP 12, 30-MHz ref. Center: 3.5 GHz (FSEA) 7 GHz (FSEB)	IF Level
18	YIG tuning voltage, high frequency	TP 13, 30-MHz ref. Center: 3.5 GHz (FSEA) 7 GHz (FSEB)	Tuning Voltage YIG
19	Cal. generator level	TP 1, Cal. gen. -40 dBm	Cal Level
20	Cal. generator control voltage	TP 0, Cal. gen. 0 dBm	Cal Level Control
21	TC/OCXO tuning voltage	TP 8	

Individual polling of the test signals without the associated instrument setting is also possible using a service function:

```
SERVICE FUNCTION
   2.10.1.X
```

X = Number of test point

The status register provides further information on the functioning of the module:

Status bit	Monitoring function	Meaning	Condition
#0	PLL of sweep synthesizer	1: Sweep synthesizer unlocked	
#1	120-MHz PLL	1: Reference oscillator unlocked	
#2	reserved		
#3	YIG control loop	1: Main loop unlocked	
#4	Option identification OCXO	1: OCXO is provided	Option FSE-B4 provided
#5	OCXO, oven temperature	0: oven cold 1: Oven is at operating temperature	Option FSE-B4 provided
#6	LCA status	0: Programming faulty 1: Programming finished	
#7	Frequency offset of YIG oscillator	0: offset > 0 1: offset <0	

The status byte is polled by means of a service function.

```
SERVICE FUNCTION
   2.10.2
```

It is indicated in the following format:

MSB							LSB
X	X	X	X	X	X	X	X

7.3.2 Error in the FTP

7.3.2.1 Error in the Transputer Download

If an error occurs during the download, the 20-MHz reference output X145 should be checked first, since the clock for the level and frequency transputer is derived from this signal. The 20-MHz signal must be immediately available after switching on of the instrument in order for the test program GR_CHECK.EXE (see service documents GRAPHICS) to provide useful results for the two transputers in the analog unit.

7.3.2.2 Error in the LCA Download

If the error message *Download FRAMCON.BIN Failed* occurs in the LCA download, the file FRAMCON.BIN on the hard disk should be checked. If no download is possible although the file is correct, there is an error in the frequency transputer or LCA.

7.3.2.3 Error in the Serial Interface

If the modules controlled by the frequency transputer can no longer be properly addressed, this may point to an error in the serial interface. The list Hardware Options in the info menu shows the modules identified by the instrument. If a module is missing, there is probably an error in this module. If all modules or the module FRAC SYN is missing, there is a fault on the FRAC SYN, or the interface is inhibited by another module. By withdrawing individual modules, the fault can be further located.

Note: *The modules FRAC SYN and DETECTOR and the connection of the 20-MH reference must remain inside the instrument!*

7.3.3 Error in the Reference Frequency Conditioning

The following symptoms may indicate an error in the reference frequency conditioning:

- Error in Transputer Download of the modules FRAC SYN and DETECTOR (see 7.3.2.1).
- Error in test functions 1-7
- Error message *Synthesizer Unlock.*

On occurrence of the error message *Synthesizer Unlock* the status register can be read out to determine whether a control loop on the FRAC SYN module has caused this message and, if so, which one.

7.3.3.1 Absolute Frequency Accuracy

Error with test function 5 or Synthesizer Unlock, Statusbit #1=1, or poor accuracy with Marker Count.

a) Instrument is operated with internal reference:

- Option B-4 not provided:

Check the reference level using test function 1.

- Error with test function 1: TCXO on the FRAC SYN module faulty.

- Option B-provided:

Check the reference level using test function 2.

- Error with test function 2: Measure voltage at X140-C23: 12 V ± 0.5 V
if voltage is wrong, voltage regulator on FRAC SYN faulty,
otherwise check OCXO level at X148 → LOW PHASE NOISE X128.

If the reference level is okay, check the frequency with the frequency counter at the rear-panel output, if necessary perform adjustment according to section 7.4.1.
If the error cannot be eliminated by a readjustment, there is an error in the 120-MHz PLL.

a) Instrument is operated with external reference:

- Error message Synthesizer Unlock: Check external reference signal and setting on the FSE. If the error message still occurs, check reference level using test function 3. In the case of an error, there is a fault in the external reference divider. Check according to section 7.4.1.2.

7.3.3.2 Error in the 120-MHz Reference

Error with test function 4 Check signal at X144. → Output amplifier faulty.
Resulting error: 2nd and 3rd LO not synchronous.

7.3.3.3 Error in the Reference Output

- Error with test function 7 Check reference output at rear panel.
→ Output amplifier or switchover faulty.

7.3.4 Error in the Cal. Generator

If a calibration is not possible or an absolute level error occurs after calibration, there may be a fault in the cal. generator.

- Error with test function 19 Check level at X146 (see 7.4.2).

- Error with test function 20 Level control faulty (see 7.4.2).

7.3.5 Error in the YIG Control Loop

Errors in the YIG control loop can also be caused by faulty circuit parts of the RF MODULE or LOW PHASE NOISE (only with mod. 30 or Option B-4). Therefore, the functioning of the sweep synthesizer on the FRAC SYN module should be checked first.

7.3.5.1 Error in the Sweep Synthesizer

Error message Synthesizer Unlock (Statusbit #0=1), or error with test function 8 to 11:

- Error with test function 8: Check level at X142.
  Nominal value: 485 MHz (500 MHz with FSEB), 10 to 14 dBm

  In the case of an error, there is a fault in the VCO or output amplifier.

- Error with test function 9: Check frequency at X142. If the VCO has not locked in, there is a fault in the PLL, otherwise fault in the VCO.

- Error with test function 10: Check level at X142.

  Nominal value: 685.5 MHz (659,9 MHz for FSEB), 10 to 14 dBm

  In the case of an error, there is a fault in the VCO or output amplifier.

- Error with test function 11: Check frequency at X142. If the VCO has not locked in, there is a fault in the PLL; otherwise error in the VCO.

If the synthesizer functions properly during static operation, check sweep function according to. 7.4.3.

7.3.5.2 Error in the YIG-PLL

Error message Synthesizer Unlock (Statusbit #3=1) or error with test function 12 to 17.

- Error with test function 12, 15: Error in reference frequency conditioning.
  Internal 30/60-MHz reference faulty.

- Error with test function 13, 16, 17 IF level at X143 too low.→ check RF MODULE X134.
  If the IF level is okay, there is a fault in the IF amplifier.

- Error with test function 14 18 If test functions 12, 13 and 15, 16 are okay, check static YIG adjustment. → RF MODULE

If no error occurs during static operation, the dynamic YIG adjustment should be checked.
→ RF MODULE

7.4 Testing the Specifications

The specifications are checked inside the instrument.

7.4.1 Reference Frequency

7.4.1.1 Internal Reference

Testing and Adjustment of the internal reference frequency is performed after a warm-up time of at least 30 minutes.

Test setup:

- Set FSE to internal reference.
- Measure level at the socket REF INT/EXT at the rear panel. > 10 dBm
- Connect frequency counter to socket REF INT/EXT.

7.4.1.1.1 Operation without OCXO

Measurement and adjustment:

- Measure signal at reference output. Frequency: 10 MHz ± 10 Hz

If the frequency is out of tolerance, the reference oscillator (TCXO) can be adjusted using a service function and the new value stored in the EEPROM.

SERVICE FUNCTION 2.10.20.X.0	Vary reference setting. X = 0 to 4095

SERVICE FUNCTION 2.10.20.X.1	Store reference setting. X = 0 to 4095

7.4.1.1.2 Operation with OCXO

Messurement and adjustment:

- Check OCXO signal at LOW PHASE NOISE, X128. Level TTL
- Measure signal at reference output. Frequency: 10 MHz ± 1 Hz

If the frequency is out of tolerance, the reference oscillator (OCXO) can be adjusted using a service function and the new value stored in the EEPROM of the LOW PHASE NOISE module.

SERVICE FUNCTION 2.10.20.X.0	Vary reference setting. X = 0 to 3300

SERVICE FUNCTION 2.10.20.X.1	Store reference setting. X = 0 to 3300

7.4.1.2 External Reference

Test setup:

- Connect signal generator 1 MHz, 0 dBm to socket REF INT/EXT.
- Connect reference output of signal generator to RF input of FSE.

Measurement:

Setting on the FSE:

CENTER	1000 MHz
SPAN	0 MHz
REF LEVEL	10 dBm
MARKER	COUNT
COUNTER RESOL	0.1Hz
REFERENCE	EXTERN, 1 MHz

- Marker display: 10 MHz ± 1 Hz
- Repeat measurement with transmitter frequency 2.3 to 16 MHz and respective FSE setting.

7.4.2 Cal Generator

Test setup:

- Connect power meter to X146.

Measurement and adjustment:

Setting on the FSE:

CENTER	120 MHz
SPAN	10 kHz
REF LEVEL	- 40 dBm
SETUP→SERVICE→INPUT CAL	

- Adjust level at X146 to -40 dBm ± 0,1 dB using R22.
  R22 is accessible through a hole in the locking bar from the bottom of the instrument.

Final adjustment in the instrument:

- Set signal generator 120 MHz to - 40 dBm ± 0.05 dB using the power meter.
- Connect signal generator to RF input of FSE.
- Switch to INPUT RF on FSE and measure level at 120 MHz.
- Switch to INPUT CAL and adjust R22 such that the level value of the previous measurement is obtained again.

7.4.3 Sweep Synthesizer

Test setup:

- Connect spectrum analyzer to X142.

Measurement:

Setting on the FSE:

START	0 Hz
STOP	1798 MHz (2558 MHz for FSEB)
SWEEPTIME	10 s
SWEEP	SINGLE SWEEP

- Trigger Single Sweep.
- The signal on the spectrum analyzer sweeps from 485.71 MHz (500.0875 MHz) to 685.4889 MHz (659.925 MHz).

7.4.4 YIG Control Loop

7.4.4.1 Checking the Phase Detector

Test setup:

- Connect signal generator to X143 and apply 29 MHz, -15 dBm.

Measurement:

Setting on the FSE: Call test function 14.

- The voltage indicated on the display reads < -2.5 V.
- Change transmitter frequency to 31 MHz.
- The selftest voltage is > +2.5 V.

7.4.4.2 Checking the Coarse Tuning

Test setup:

- Connect oscilloscope to X140.C15.

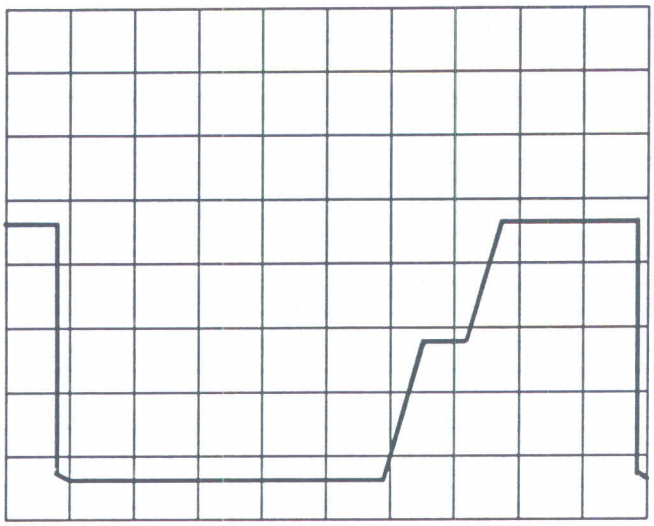
Measurement:

Setting on the FSE:

START	0 Hz
STOP	3500 MHz (7000 MHz for FSEB)
SWEEPTIME	5 ms

- Measure the voltage at X140.C15:

Start value:	1.39 V (0.52 V for FSEB)
Final value:	9.63V (8.76 V for FSEB)



7.4.4.3 Checking the Sweep Output

Test setup:

- Connect oscilloscope to SWEEP socket at the rear panel.

Measurement:

Setting on the FSE: see 7.4.4.2.

- Measure voltage at rear-panel socket:

Start value	0 V
Final value	+10 V

7.5 External Interfaces

Pin	Name	Input/ Output	Origin/destination	Value range	Signal description
A1	READY	A		TTL	Ready signal from FTP
A3	M_STROBE	A	LOW PHASE NOISE	TTL	Strobe for M-divider
B3	Det_Dis	A	DETECTOR	TTL	Detector Disable
A5	GND_D	B		0V	Ground digital
B5	GND_D	B		0V	Ground digital
C5	GND_D	B		0V	Ground digital
A6	+5V_D	E		+5,2 V ± 0,05V	+5 V digital
B6	+5V_D	E		+5,2 V ± 0,05 V	+5 V digital
C6	+5V_D	E		+5,2 V ± 0,05 V	+5 V digital
B7	LINK_F>P	A	DETECTOR	TTL	Link to PTP
B8	LINK_P>F	E	DETECTOR	TTL	Link from PTP
B9	LINK_F>G	A	GRAPHICS	TTL	Link to GTP
A10	FTP_CLK	A		TTL	Interface of frequency transputer, clock
B10	LINK_G>F	E	GRAPHICS	TTL	Link from GTP
C10	FTP_DAT	A		TTL	Interface of frequency transputer, data
A11	FTP_STRA	A		TTL	Interface of frequency transputer, address strobe
B11	LINK2_F>P	A	DETECTOR	TTL	Link 2 to PTP
C11	FTP_DATR	E		TTL	Interface of frequency tansputer, data
A12	FTP_CLKR	E		TTL	Interface of frequency transputer, clock
B12	LINK2_P>F	E	DETECTOR	TTL	Link 2 from PTP
C12	FTP_STRD	E		TTL	Interface of frequency transputer, data strobe

Pin	Name	Input/ Output	Origin/Destination	Value range	Signal description
A13	TRAC_F	A	TRACKING GENERATOR	0 to 10 V	Tuning voltage tracking generator
C13	Tune_Pres	A	MW CONVERTER, PRESELECTOR	0 to - 10 V	Tuning voltage preselection
A14	TRAC_P	A	TRACKING GENERATOR	0 to 10 V	Freq, resp. correction tracking generator
B14	Sweep	A		0 to 10 V	Sweep output on rear panel
A15	Cal_Amp1	A	IF FILTER	0 to 10 V	Freq. resp. correction on IF FILTER
B15	Det_Hold	A	DETECTOR	TTL	Hold measured value
C15	PRETUNE	A	RF MODULE	0 to 10 V	YIG coarse tuning
B16	Det_Mem	A	DETECTOR	TTL	Read measured value
C16	GNDDAC	A		0 V ± 10 mV	Reference for tuning volt.
A17	YIGCON	A	RF MODULE	- 15 V to + 15 V	YIG fine tuning
B17	Det_Rst	A	DETECTOR	TTL	Meas. value transfer, detector reset
B18	Sweep_Hold	E		TTL	Stop sweep
B19	Error2	A		open collector	FTP error
C19	GND_YIG	A	RF MODULE	0V	Reference ground for YIGCON
B20	LINK_F>A	A		TTL	LINK3
B21	LINK_A>F	E		TTL	LINK3
A22	LO_unlock	A	DETECTOR	open collector	Synthesizer unlocked
C22	OCXOTUNE	A	LOW PHASE NOISE	0 to 8 V	Tuning voltage OCXO Option
C23	+12V_OV	A	LOW PHASE NOISE	+12 V	Supply voltage OCXO
A24	INTRES	E	DETECTOR	TTL	Reset error message
B24	ANALYSE	E		TTL	Analysis line FTP
C24	OPT	E	LOW PHASE NOISE	TTL	Option identification
A25	ADCMUX	A		-5 V to +5V	Test channel for selftest
C25	OVEN_COLD	E	LOW PHASE NOISE	0 to 5V	Status display of OCXO

Pin	Name	Input/ Output	Origin/Destination	Value range	Signal description
A26	ADCGND	B		0 V	Reference ADCMUX
C26	F_SDA	E		TTL, 100 kHz	I^2C bus
A27	TRESET	E	GRAPHICS	TTL	Transputer reset
C27	F_SCL	E		TTL, 100 kHz	I^2C bus
C28	+28V	E		+28 V ± 1 V	Supply
A29	-15V	E		-15 V ± 0.1V	Supply
B29	-15V	E		-15 V ± 0.1 V	Supply
C29	-15V	E		-15 V ± 0.1 V	Supply
A30	+15V	E		+15 V ± 0.1 V	Supply
B30	+15V	E		+15 V ± 0.1 V	Supply
C30	+15V	E		+15V ± 0.1 V	Supply
A31	+5V_A	E		+5.5 V ± 0.05 V	+ 5 V analog
B31	+5V_A	E		+5.5 V ± 0.05 V	+ 5 V analog
C31	+5V_A	E		+5.5 V ± 0.05 V	+ 5 V analog
A32	GNDA	B		0 V	Ground analog
B32	GNDA	B		0 V	Ground analog
C32	GNDA	B		0 V	Ground analog
X141	INTPOL	E	LOW PHASE NOISE	30.3 to 43.75 MHz, 0 dBm	divided FRACSYN signal
X142	FRACSYN	A	RF MODULE or LOW PHASE NOISE	475 to 700 MHz, 10 to 14 dBm	Interpolation synthesizer
X143	IFSYN	E	RF MODULE	< 100 MHz, > -20 dBm	IF from YIG and comb signal
X144	REF120M	A	2nd IF CONVERTER	120 MHz, 8 dBm	120-MHz reference
X145	REF20M	A	DETECTOR	20 MHz, TTL	20-MHz reference
X146	CALINT	A	ATTENUATOR	120 MHz, -40 / 0dBm	Cal generator
X147	EXTREF	B		Input: 1.2 to 16 MHz, >-10 dBm Output: 10 MHz, >+10 dBm	external reference
X148	OCXO	E	LOW PHASE NOISE	10 MHz, TTL	Input for optional OCXO

Pin	Name	Input/ Output	Origin/Destination	Value range	Signal description
X149	YIGCON	A	RF MODULE	- 15 V to + 15 V	YIG fine tuning

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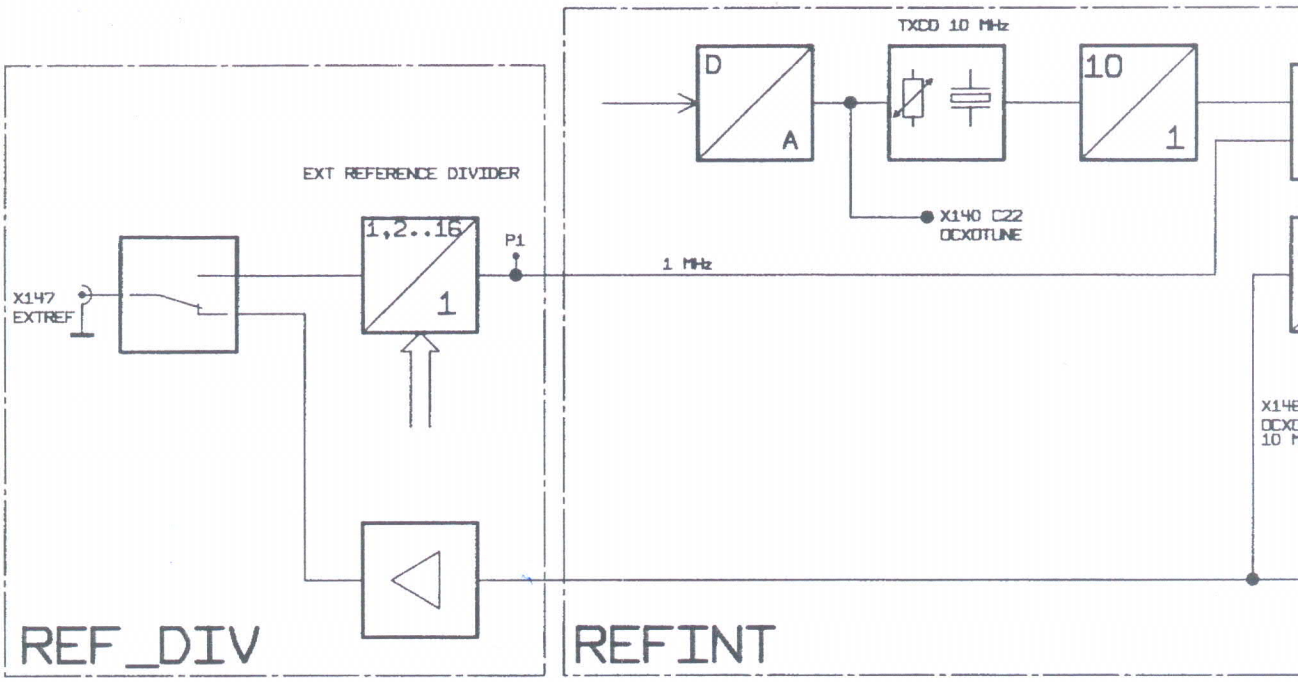
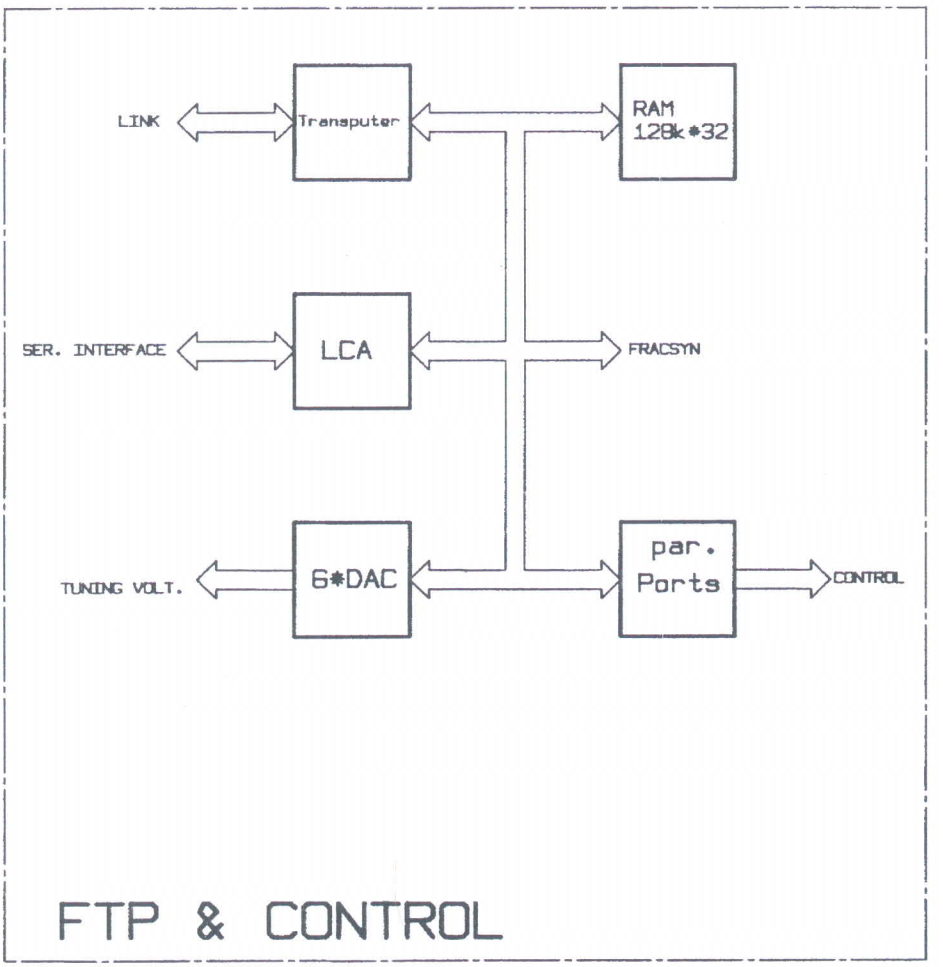
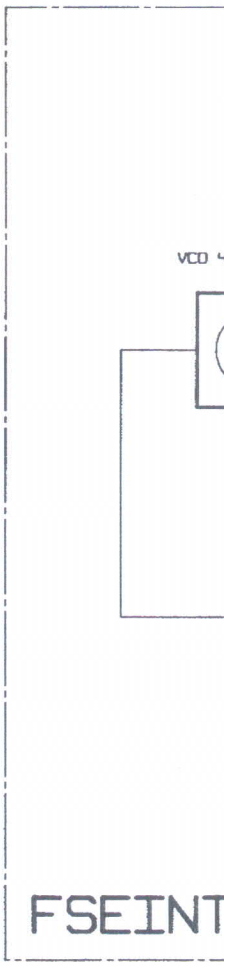
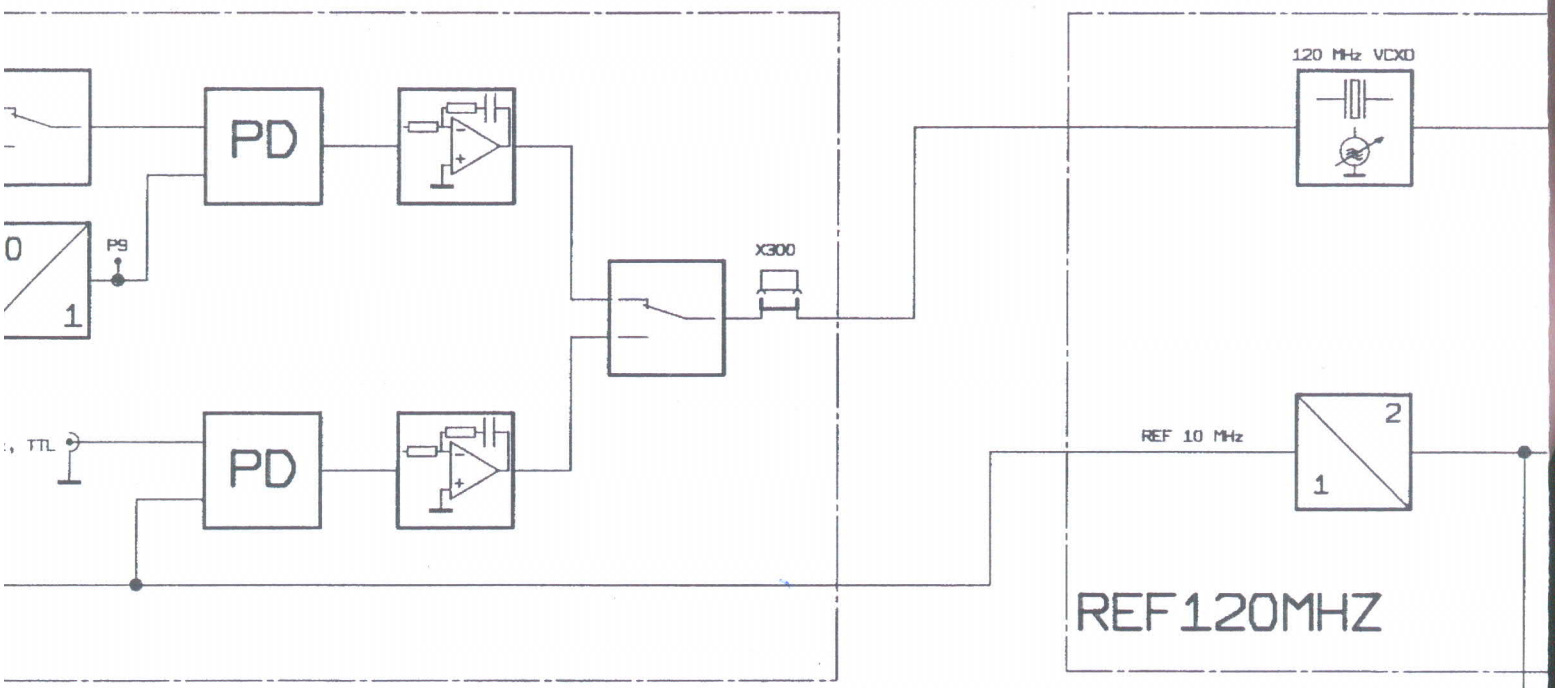
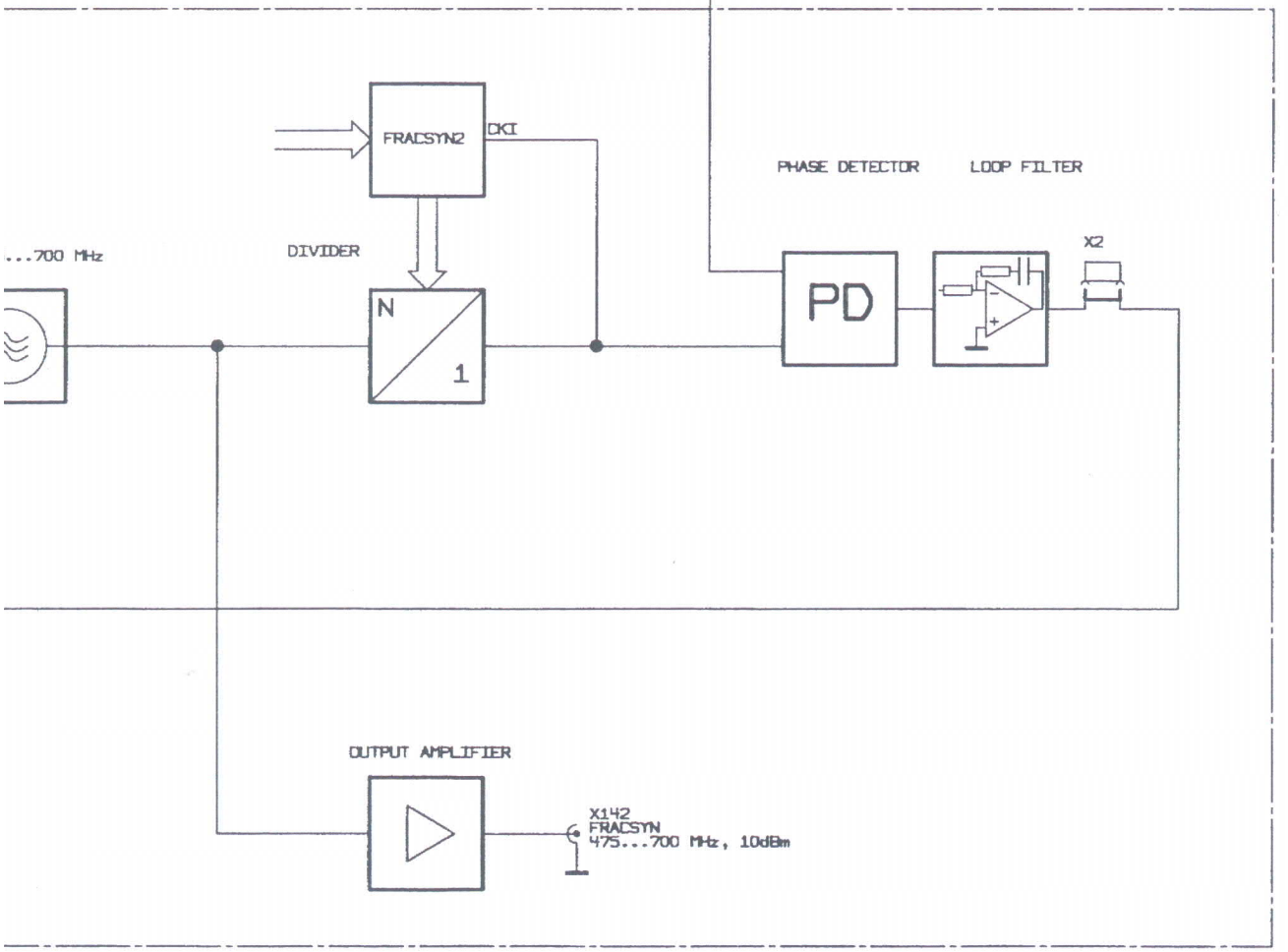




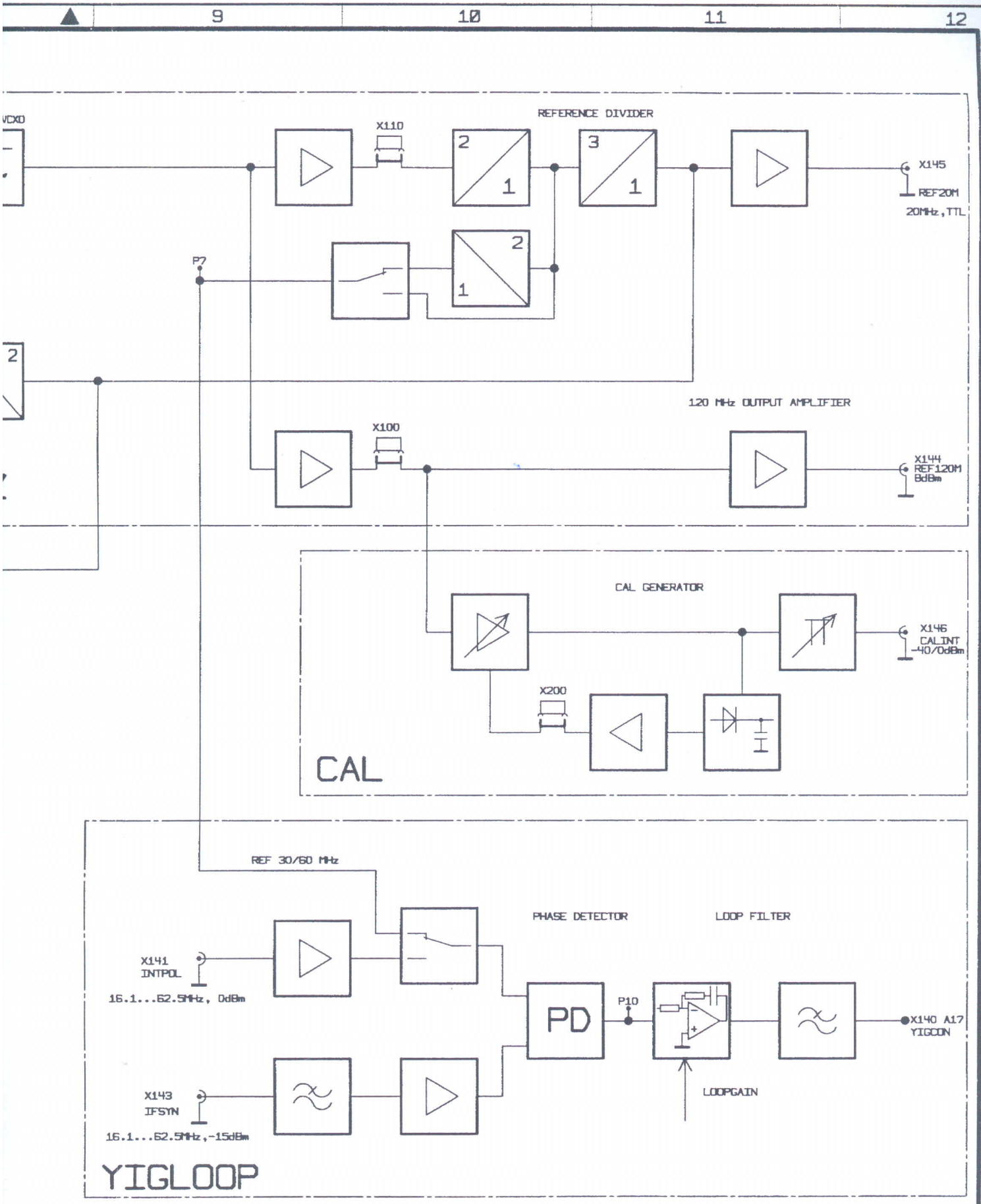






ACHTUNG: EGB!
ELEKTROSTATISCH GEFAEHRDETE BAUELEMENTE ERFORDERN EINE BESONDERE HANDHABUNG.
ATTENTION ESD!
ELECTROSTATIC SENSITIVE DEVICES REQUIRE A SPECIAL HANDLING

05/01
05
AEND.
IND.



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				GEPR.		SO	
				NORM			
				PLOTT	05.10.95		top sheet0
05	49328(75)	8.95	SO	ROHDE&SCHWARZ			ZEICHN.-NR. 1065.7512.01S
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME				BLATT-NR. 1 v. 25 BL.
				ZU GERAET FSEA			REG.I.v. 1065.6000 ERSTE Z. 1065.7512

ROHDE&SCHWARZ

SERVICE MANUAL
LOW PHASE NOISE MODULE

1066.0763.02

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7 Test and Repair Instructions

7.1 Function Description

7.1.1 Function in Unit

The low phase noise module is an expansion synthesizer with which the FSEX-30 models are equipped as standard. The FSEX-20 models can be optionally retrofitted. The module reduces the phase noise of the 1st LO by at least 20 dB. This is obtained by comparing the sampling frequency of the YIG sampler in frequency and phase with the spectrally pure 720-MHz signal of the 3rd LO (typ. -150 dBc). The sampling signal in the basic unit, the so-called Fracsyn signal, offers the required fine frequency resolution for use in case of high phase noise. This signal is frequency divided with a large factor and thus spectrally improved so that it serves merely for interpolation between two adjacent low phase noise frequencies that are spaced about 20 MHz.
The function blocks of the module are described in detail below and are as follows:

- VCO for 611 to 714 MHz which generates the low phase noise signal
- mixer to downconvert the VCO signal to the IF of 6 to 109 MHz with the 3rd LO signal
- fractional frequency divider N,F/1 for the division of the 720-Hz signal to the required IF frequency
- phase detector to generate the control voltage for the VCO by means of the IF signals from the mixer and fractional frequency divider
- frequency divider 16/1 for the FRACSYN signal to generate the interpolation signal
- control block for the selftest
- interface to control the module

7.1.2 Description of Function Blocks

VCO with LO amplifier

see sheet 7 of circuit diagram

At spans <30 MHz the VCO switched on by VCO_ ON=H outputs the sampling signal SAMPL for the YIG sampler. The switchable amplifier for the FRACSYN signal is blocked in this mode with FRA_ON=L. The VCO is tuneable between 611 and 714 MHz with UVAR= 2 to 13 V. The VCO signal is available for the output amplifier with 8 dBm at the internal interface FRAADD and as an LO signal for the mixer with 18 dBm at the internal interface LOMIX. The rectified LOMIX signal LOMES serves for the selftest.

Mixer

see sheet 6 of circuit diagram

This circuitry performs the downconversion of the VCO signal to the IF of 6 to 109 MHz with the aid of the 720-MHz signal of the 3rd LO, band-limitation to suppress unwanted frequencies and conversion to the TTL signal PDVCO for the phase detector. The 720-MHz signal is decoupled via an isolating amplifier and is made available as REFDIV with 0 dBm for the reference divider. The rectified signals from the mixer RFMES and IFMES are used in the selftest of the instrument.

Fractional frequency divider

see sheet 4 of circuit diagram

The fractional frequency divider generates from the 720-MHz signal of the 3rd LO the reference signal between 6 and 109 MHz for the phase detector. The whole integer frequency division N=7 to N=120 is made with the ECL driver IC 10E016. Whole integer division factors would be too large for the frequency step of the low phase noise output signal so that intermediate steps N;F with F= 10/16, 2*10/16, 3*10/16..... are necessary. These are generated using the so-called fractional N technique. For example dividing by 7 over fifteen reference periods and by 8 over one reference period yields an average division factor of $7\ ^{1}/_{16}$. An increment adder controls the division factor by counting up the factor F with the reference periods until a carry occurs and then applying the division factor N + 1 to the frequency divider by means of a multiplexer. The TTL signal PDREF is taken to the phase detector after level conversion. The DC signal DIVMES derived from the TTL signal is again used for the selftest.

Phase detector

see sheet 3 of circuit diagram

To avoid the occurrence of too high comparison frequencies at the digital phase detector, the frequencies are divided up into four signals shifted 90° to one another and applied to four identical phase detectors. The output voltages are added up at the integrator input. The DC signal FGAZ derived from the phase detector output signal serves for the selftest.

FRACSYN divider

see sheet 5 of circuit diagram

The main loop of the 1st LO (YIG synchronization) operates in the basic unit with a reference frequency of 30 (60) MHz. For operation with the low phase noise module the Fracsyn frequency divided through 16 for interpolating between the possible low phase noise frequencies serves as the reference frequency for the main loop. An ECL frequency divider MC 12096 divides the Fracsyn frequency at first by 8 and then by 2 after conversion to TTL level.
The circuit for generating the Fracsyn also contains a switchable amplifier which isolates the Fracsyn signal from the YIG sampler in the low phase noise mode.

Control block

see sheet 8 of circuit diagram

The selftest block consists mainly of a multiplexer which switches the buffered and amplified test voltages to the A/D converter input as well as a window comparator with memory FF for generating the UNLOCK interrupt.

Interface

see sheet 9 of circuit diagram

The interface block incorporates an address decoder for the module addresses 32 and 33, an EPROM as well as a shift register for the module setups.

7.2 Measuring Equipment and Accessories

Item	Type of equipment	Required characteristics	Suitable R&S unit	Order No.	Use
1	Digital multimeter	1 mV to 100 V 0.1 mA to 1 A	UDS5	349.1510.02	
2	Frequency counter	Accuracy >$1*10^{-8}$			
3	Signal generator	100 kHz to 3500 MHz	SMHU	835.8011	
4	3-dB coupler	Decoupling >20 dB; 1 to 3500 MHz			
5	Attenuator pad	6 dB	DNF	274.4110.50	
	Spectrum analyzer	100 kHz to 8000 MHz	FSM	1020.7020.52	
7	Power meter	100 kHz to 3500 MHz	URV5 NRV-Z	349.8012.02	
8	Network analyzer	300 kHz to 3500 MHz			

7.3 Troubleshooting

Six test voltages and an interrupt signal are provided for locating faults on the low phase noise module. The selftest is to be carried out at settings at which the low phase noise frequency attains its maximum or minimum value.

Instrument settings:

	Span	Zero	
For 3.5-GHz model:	Center frequency	598 MHz	LOW PHASE: 710 MHz
	Center frequency	668 MHz	LOW PHASE: 630 MHz
For 7-GHz model:	Center frequency	518 MHz	LOW PHASE: 710 MHz
	Center frequency	818 MHz	LOW PHASE: 630 MHz

7.3.1 Test Functions

TEST-FUNCTION	DESCRIPTION	SETTING	VALID VALUE RANGE	ERROR MESSAGE
0	Module test, test functions 1 to 7	All test functions		LOW-PHASE-NOISE-ERROR
1	Local level for mixer, VCO signal	LOMES	V > 1.5 V	LO-LEVEL
2	RF level for mixer, 720-MHz reference signal	RFMES	V > 1.5 V	RF-LEVEL
3	720-MHz level at divider input	REFMES	V > 1.5 V	LEVEL DIVIDER
4	Mixer output level	IFMES	V > 1.5 V	IF-LEVEL
5	Fractional frequency divider output signal	DIVMES	V=2.5 V ±0.5 V	FRAC-DIVIDER
6	PLL lock indication	FGAZ	V= 0 V ±2 V	PLL-ERROR
7	PLL interrupt	LOCK	V=2.5 V ±0.5 V	UNLOCK

Service function: The test signals can be polled per service function independent of the instrument setting:

2.13.1.X X: test function number

7.3.2 Fault Description

A faulty low phase noise module causes as a rule at spans of <30 MHz incorrect frequency display of the test signal or the signal not being reproduced at all or an unstable display.

Error message	Causes
LO-LEVEL	Occurs in conjunction with other error messages (IF-LEVEL, FGAZ). VCO does not oscillate or with too low level (switch-off?) LO amplifier
RF-LEVEL	Produces further error messages. 720-MHz signal of the 3rd LO missing or too small RF amplifier
LEVEL DIVIDER	Same as RF-LEVEL
IF-LEVEL	Usually resulting from previous error messages, otherwise IF amplifier
FRAC DIVIDER	Usually resulting from the error message RF-LEVEL, otherwise data transmission problem (programming of 10E016), ECL/TTL converter
PLL-ERROR	Usually resulting from previous error messages, otherwise test phase detector.

7.4 Tests and Adjustments

Connect SMHU to analyzer input.
Check for correctness of the displayed frequency in the frequency range 598 to 668 MHz in 1-MHz steps at 10-MHz span.
Check the phase noise at the limit frequencies against the data sheet using the noise marker.

7.5 External Interfaces

Pin	Name	Input/ Output	From/to	Value range	Signal description
A5	GND_D	B			Ground, digital
C5	GND_D	B			Ground, digital
A6	+5V_D	I		5.2 V ± 0.05 V	Voltage supply
C6	+5V_D	I		5.2 V ± 0.05 V	Voltage supply
A10	FTP_CLK	O	FRACSYN	TTL	Interface to frequency transputer clock
C10	FTP_DAT	O	FRACSYN	TTL	Interface to frequency transputer, data
A11	FTP_STRA	O	FRACSYN	TTL	Interface to frequency transputer, address strobe
C12	FTP_STRD	I	FRACSYN	TTL	Interface to frequency transputer, data strobe
A22	LO_UNLOCK	O	Detector	open collector	Interrupt signal
C22	OCXOTUNE	O	FRACSYN	0 to 8 V	Tuning voltage OCXO option
C23	+12V_OV	O	FRACSYN	+12 V	DC supply voltage OCXO
C24	OPT 1	I	FRACSYN	TTL	Option identification
A25	ADCMUX	O	Detector	-5 V to +5 V	Test channel
C25	OVEN_COLD	C25	Detector	0 to 5 V	Cold : V< 0.4 V Warm: V > 2.8 V
C26	F_SDA	I	FRACSYN	TTL, 100 kHz	I^2C bus, data
C27	F_SCL	I	FRACSYN	TTL, 100 kHz	I^2C bus, clock
A29	-15V	I		-15 V ± 0.1 V	Voltage supply
C29	-15V	I		-15 V ± 0.1 V	Voltage supply
A30	+15V	I		+15 V ± 0.1 V	Voltage supply

Pin	Name	Input/ Output	From/to	Value range	Signal description
C30	+15V	I		+15 V ± 0.1 V	Voltage supply
A31	+5V_A	I		+5.5 V ± 0.05 V	Voltage supply
C31	+5V_A	I		+5.5 V ± 0.05 V	Voltage supply
A32	GNDA	B		0 V	Ground, analog
C32	GNDA	B		0 V	Ground, analog
X128	OCXO_IN	O	FRACSYN	TTL, 10 MHz	OCXO reference signal
X123	SAMPL	O	YIG sampler, RF module	611 to 714 MHz, 10 dBm for LOW PHASE 470 to 700 MHz for FRACSYN operation	Sampling mixer
X122	FRACSYN	I	FRACSYN	470 to 700 MHz, 8 dBm	Fracsyn frequency
X121	INTPOL	O	FRACSYN	470 to 700 MHz/16 ECL	Phase comparison signal for main loop
X125	REF720MHz	I	2nd IF Converter	720 MHz, 10 dBm	3rd LO

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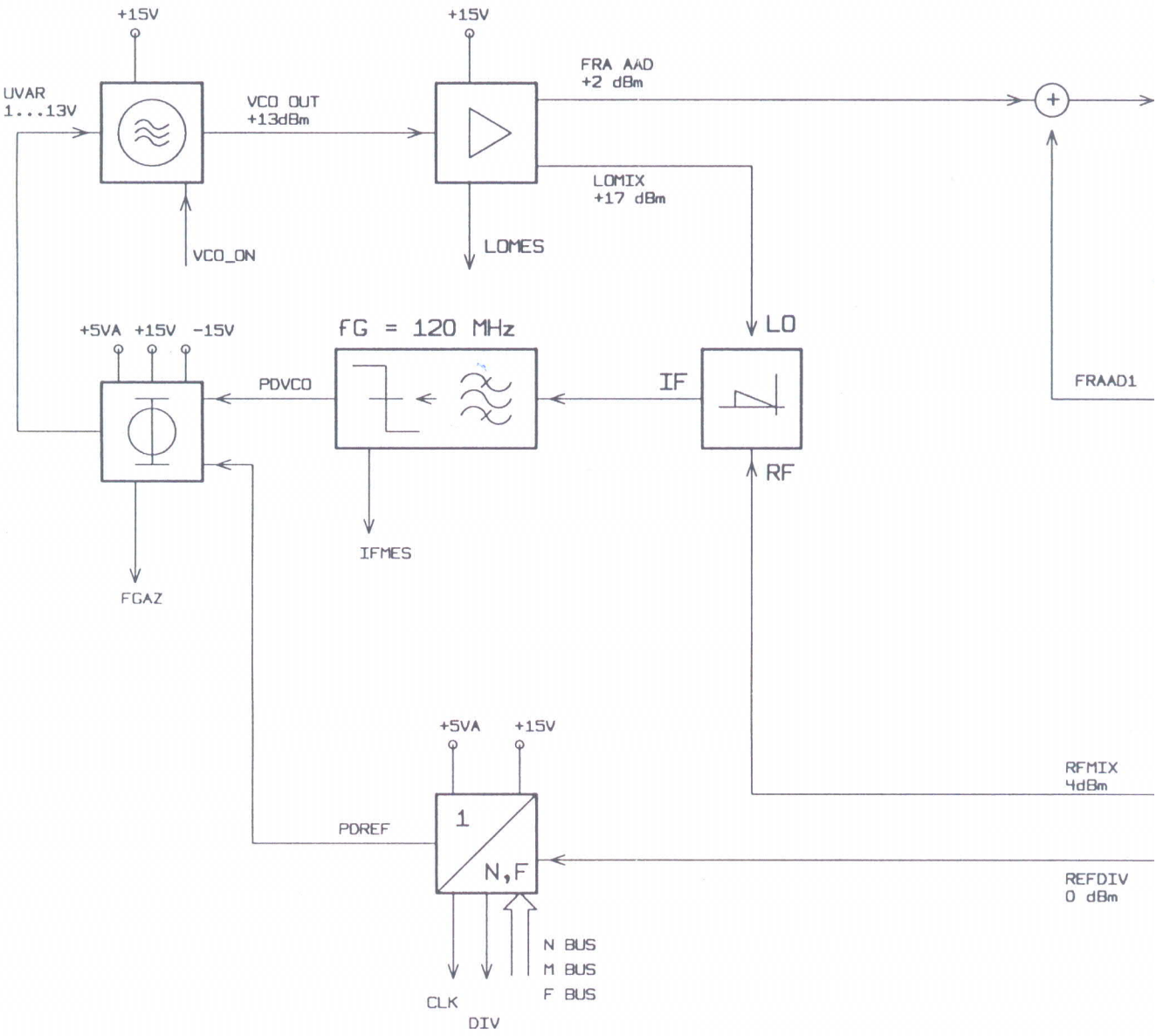

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ELEKTROSTATISCH GEFAEHRDETE BAUELEMENTE ERFORDERN EINE BESONDERE HANDHABUNG.
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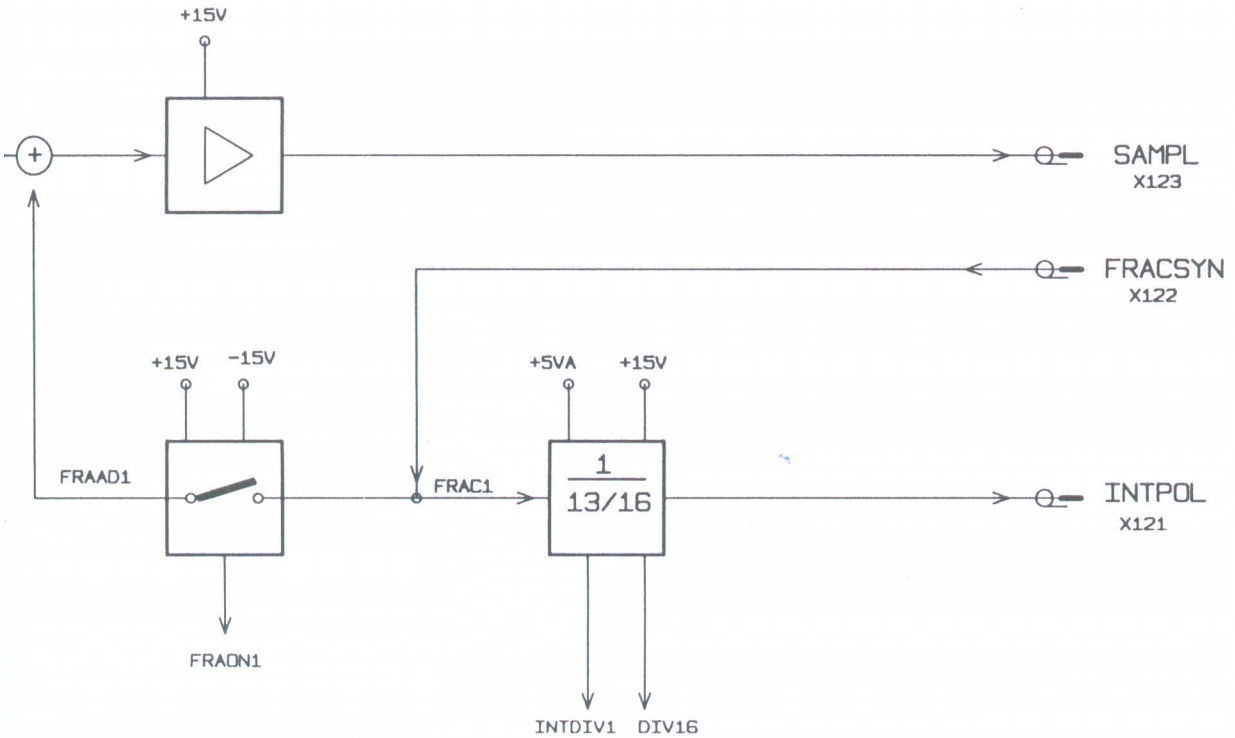
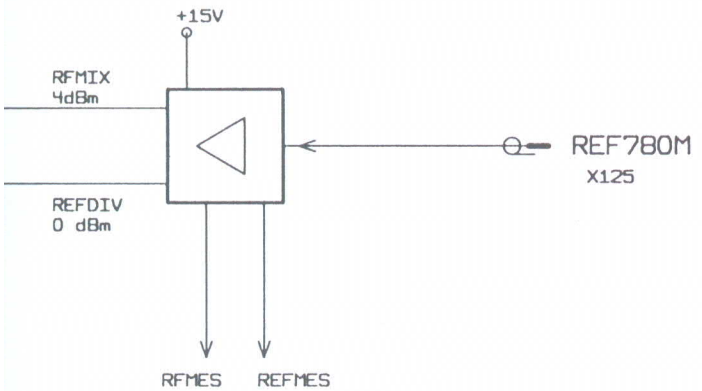
ELECTROSTATIC SENSITIVE DEVICES REQUIRE A SPECIAL HANDLING





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				NORM			top sheet0
				PLOTT	24.07.95		
03/03	49328(49)	13.06.95	NL	ROHDE&SCHWARZ			ZEICHN.-NR. 1066.0763.01S
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ZU GERAET FSEA			BLATT-NR. 1 v.9 BL.
							REG.I.V. 1065.6000 ERSTE Z. 1065.6000

ROHDE&SCHWARZ

SERVICE MANUAL
2ND IF CONVERTER

1065.7012.02

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7 Test and Repair Instructions

7.1 Circuit Description

7.1.1 Function in Unit

The 2nd IF Converter module converts the second IF (1st IF for FSEM) at 741.4 MHz of the RF Module (MW Converter for FSEM) to an IF of 21.4 MHz. To perform this function, the following components are provided on the converter:

- IF amplifier and 10-MHz resolution filter
- mixer for converting 741.4 MHz to 21.4 MHz
- PLL for generating the 3rd LO signal
- frequency multiplier and LO amplifier for the 2nds LO signal
- TV demodulator (option FSE-B3)

7.1.2 Description of Block Diagram

The 2nd IF Converter is controlled via the serial interface of the frequency transputer.

Signal path

The module has two IF inputs for the various RF sections of the individual FSE modules. The signal of the RF Module (FSEA, FSEB) is amplified by 16 dB, whereas the signal of the MW Converter (FSEM) is taken directly the input selector. A power splitter distributes the IF signal to the broadband IF output and the 10-MHz resolution filter. This filter is made up of two sections with 3 circuits each. An isolating amplifier buffers the two sections. An overload detector s provided in the broadband signal path.
After the 3rd mixer, there follows an IF amplifier and a switchable attenuator for gain matching in the various RF ranges.
At resolution bandwidths ≤ 3 MHz a 5-MHz bandpass is switched into the signal path.

LO processing

A 720-MHz VCO is synchronized to the sixfold of the 120-MHz reference with the aid of a PLL.
The 720-MHz signal is used as the LO for the 3rd mixer, reference for the module Low Phase Noise and as input signal for the 720-MHz comb generator. The 3.6-GHz line is filtered out and amplified for the 2nd LO.

EEPROM

The EEPROM contains setting and correction values for the module so that the module can be exchanged without adjustments. Some of the settings can be changed by means of the service functions and stored in the EEPROM. if required.

The key data are:

- thresholds for the overload detectors
- tuning of the 720-MHz VCO
- gain error of the module

7.2 Measuring Equipment and Accessories

Item	Type of equipment	Required characteristics	Suitable R&S unit	Order No.	Use
1	Digital multimeter	1 mV to 100 V 0.1 mA to 1 A	UDS5	349.1510.02	7.4.2
2	Signal generator	100 kHz to 800 MHz	SMG		7.4.1 7.4.2
3	Signal generator	100 kHz to 3600 MHz	SMHU	835.8011	7.4.2
4	3-dB coupler	Decoupling >20 dB; 1 to 1000 MHz			7.4.2
5	Spectrum analyzer	100 kHz to 4000 MHz	FSB		7.4.1 7.4.2
6	50-Ω termination, SMB				7.4.2

7.3 Troubleshooting

Any fault on the 2nd IF Converter can be clearly located with the aid of the following the description. A module found faulty should be replaced.

Module replacement

- The module does not need to be adjusted in the unit.
- The automatic selftest should run error-free after a replacement. This should be followed by a total calibration.

7.3.1 Selftest

Within the selftest 16 voltages can be measured. The voltages are measured automatically at specific settings and checked if they within a given tolerance window.

Note: *A prerequisite for the automatic selftest is that the modules RF Module, Frac Syn and Detector are fully operational. To avoid the occurrence of inappropriate error messages the automatic test for the complete unit will be aborted after detecting the first out-of-tolerance condition. For locating the fault more accurately test functions in the board test menu can be called up manually and run using external signals.*

The basic setting for the 2nd IF Converter and for the test functions are performed automatically. The voltages measured in the selftest and the permissible tolerance limits are shown on the analyzer display.

Basic setting:	Center:	120 MHz
	Span:	zero
	RF attenuation:	0 dB
	Cal. Generator:	0 dBm

Table 7-1 Test functions:

Test funct.	Designation	Setting	Error message
0	Test 1 to 14 Module test	Test 1 to 14	
1	120-MHz comb generator	TP 7	Level 120 MHz SRD
2	VCO test	TP 6	Level 720 MHz PLL
3	720 MHz output	TP 5	Level 720 MHz Output
4	Lock test	TP 4	Tuning Voltage AC
5	Tuning test	TP 10	Tuning Voltage DC
6	720-MHz comb generator	TP 2	Level 720 MHz SRD
7	Operating point of LO driver input stage	TP 3	Bias 2nd LO Driver
8	Operating point of LO driver output stage	TP 8	Bias 2nd LO PA
9	Level of 3rd LO	TP 9	Level 3rd LO
10	Operating point of IF amplifier 741.4 MHz	TP 11	Bias 2nd IF Amp.
11	Level at module input	TP 0	IF 741.4 MHz Level
12	Level at module input - 10 dB	TP 0 RF Att. 10 dB	RF Attenuator
13	Mixer test	TP 0 Center 0 Hz	1st Mixer
14	Level at module output	TP 1	IF 21.4 MHz Level
		TP 12 to TP 15 reserved for TV option	

Test signals can also be queried without the associated setting by using the service function:

```
SERVICE FUNCTION
    2.12.1.X
```

`X = Number of the testpoint`

7.3.2 Fault in LO Section

The following symptoms can point to a fault in the LO processing circuit on the module 2nd IF Converter:

- error message *Synthesizer unlock*
- error message in selftest with test functions 1 to 9
- frequency offset of the displayed signal or LO at sweep start

If the error message *Synthesizer unlock* is caused by the module 2nd IF Converter, the frequency of the displayed signal is most probably incorrect. Spurious lines may well occur.
As next step the selftest should be called up to localize the fault more accurately.

7.3.2.1 Frequency Readout Error

Error with test function 1:	Check 120-MHz reference → FRAC SYN, X144, if the reference is in order, fault in 120-MHz comb generator.
Error with test function 2:	Call up test function 3. If the test value is outside tolerance, the VCO is defective, otherwise the LO amplifier in PLL path is faulty.
Error with test function 4 and 5:	VCO not synchronized or tuning voltage outside tolerance. Check VCO tuning (→ section 7.4.1.1).

7.3.2.2 Level Readout Error

Error with test function 3:	If test function 2 is error-free, output or buffer amplifier is defective, check signal at X1511.
Error with test function 6:	Fault in 720-MHz comb generator. Check signal at X151.
Error with test functions 7 and 8:	Fault in LO amplifier. Check level at X151.
Error with test function 9:	Amplifier for 3rd LO defective provided test functions 2 are without errors.

7.3.3 Fault in Signal Path

7.3.3.1 Level Error

A total calibration should be performed first when the level error is small. If the fault still occurs, it can be narrowed down by means of the error messages of the calibration or selftest. A calibration is not expedient when large level errors (>8 dB) are involved. The function of the module can be tested with the aid of the selftest functions or through measurement of the signal level at the interfaces.

Error with test function 10:	IF amplifier defective.
Error with test function 11:	Check level at X152 → RF Module or 2nd LO defective → section 7.3.2 otherwise IF amplifier or input selector defective.
Error with test function 14:	Check level at X158. Check overall gain of module.

7.3.3.2 Noise Indication too High

The possible sources of noise are:

- absolute level error
- noise figure of the 2nd IF Converter
- sideband noise of 2nd/3rd LO

It should first be checked whether the level and noise indication after the 2nd IF Converter is in order: → IF Filter, Detector.
Call test function 14 and measure level at X158. Rated value: +4 dBm ± 3 dB. In case of error, check level at module input (→ RF Module) and gain of module according to 7.4.2.1.

Terminate IF input X152 of 2nd IF Converter with 50 Ω and check noise indication according to 7.4.2.4. If the expected value is not obtained, the fault is in the signal path of the 2nd IF Converter, otherwise in the RF Module.

A high noise indication in the frequency range < 50 MHz (< 70 MHz for FSEB) can also be caused by the phase noise of the 1st and 2nd LO or by insufficient suppression of the 1st LO (→ RF Module).

Settings on FSE:
Span 0 to 100 MHz
RF ATT 0 dB
REF LEVEL -10 dBm
RBW 1 MHz

Measure the LO level with marker. If the level is within tolerance, check the noise meter with the phase noise marker. If the indication is too high, the 2nd LO should be replaced by a clean signal source(eg SMHU). If the noise indication is still too high, the fault is in the 1st LO.
Check → RF Module, Frac Syn.

7.3.3.3 Intermodulation Suppression too Low

If the intermodulation suppression is too low, it should be checked whether this is already the case at the IF output of the active RF Converter or occurs at the 2nd IF Converter or IF Filter. The IF signal is to be checked as follows:

- set the center frequency at which the error occurs.
- set ZERO SPAN, RF ATT 0 dB.
- apply two signals at the center frequency to the RF input from two generators via a 3-dB coupler. The level of the two signals should be -10 dBm, the frequency offset 100 kHz.
- measure IF signal at output X137 with spectrum analyzer of the RF Module. The intermodulation suppression should be > 55 dB.
- measure IF signal at output X158 of the 2nd IF Converter. The intermodulation suppression should be >50 dB.

7.3.3.4 Incorrect RF Overload Indication

No RF overload indication although mixer level > + 5 dBm

Overload detector to 2nd IF Converter. Check in line with 7.4.2.3.

RF overload indication at mixer level < 0 dBm

Check whether overload is caused by 1st LO. For this purpose set start frequency to > 100 MHz. If the fault disappears. the RF Module is faulty.
Check → RF Module, LO suppression.

If the fault is still present, the overload detector is defective (see 7.4.2.3).

RF overload indication permanently on also without signal

The RF OVR line is blocked by some other module.

7.4 Tests and Adjustments

Testing the module for functionality and compliance with rated values is only required after a repair or of the fault cannot be located by other means.
The specifications of the module can be checked independently of the rest of the unit. The unit merely serves for setting the functions of the module. The display unit can be used for some of the measurements. Some alignments on the module can be performed with the aid of the service functions.

7.4.1 Testing the LO Processing

7.4.1.1 3rd LO (720 MHz)

Test setup

- Apply a signal with 120 MHz ± 10 Hz, 8 dBm to X154.
- Connect spectrum analyzer to 155.

Measurement and alignment

- Call up test function 5 in menu Board Test 2nd IF Converter.

- Measure signal at X155.	Frequency	720 MHz ± 60 Hz
	Level	8 dBm ± 2 dB
- Voltage in selftest	MUX 12.10	0.5 to 2.5 V

If the VCO is out of lock or the test voltage has reached the limit values, the VCO tuning can be corrected by means of a service function and the new value stored in the EEPROM.

SERVICE FUNCTION 2.12.27.X.0	Adjusting the tuning, X=0...255
SERVICE FUNCTION 2.12.27.X.1	Storing the new value in EEPROM, X = 0...255

- If necessary, change the tuning value such that the VCO locks and the test voltage is 1.35 V (at room temperature).
- Store new value in EEPROM.

7.4.1.2 2nd LO (3.6 GHz)

Test setup

- Apply a signal with 120 MHz ± 10 Hz, 8 dBm to X154.
- Connect spectrum analyzer to 155.

Measurement

- Measure signal at X151.	Frequency	3600 MHz ± 300 Hz
	Level	> 18 dBm

7.4.2 Testing the Signal Path

7.4.2.1 Overall Gain

Test setup

- Apply a signal with 120 MHz, 8 dBm to X154.
- Apply signal with 741.4 MHz, -20 dBm to X152.
- Connect spectrum analyzer with X158.

Measurement

Settings on FSE:	Center	120 MHz
	RBW	10 MHz
- Measure signal at X158.	Frequency	21.4 MHz
	Level	- 8 dBm ± 2 dB

7.4.2.2 IF Bandwidths

Test setup

See 7.4.2.1

Measurement

Settings on FSE:

Center	120 MHz
RBW	10 MHz

Settings on spectrum analyzer:

Center	21.4 MHz
Span	40 MHz
Ref. Level	-5 dBm
Trace	Max Hold

- Sweep input signal at X152 of 721.4 to 761.4 MHz and trace out amplitude response.

  3-dB bandwidth 9 MHz to 12.5 MHz

- Switch RBW on FSE to 1 MHz, reduce span on spectrum analyzer to 10 MHz.
- Sweep input signal at X152 of 739.4 to 746.4 MHz and trance out amplitude response.

  3-dB bandwidth 4 MHz to 5 MHz

7.4.2.3 Overload Detector

Test setup

- Apply a signal with 120 MHz ± 10 Hz, 8 dBm to X154.
- Apply a signal with 741.4 MHz, -20 dBm to X152.
- Connect multimeter to X150.C20 and X150.C21.

Measurement

Settings on FSE:

Center	120 MHz
Sweep	Single Sweep

- An interrupt reset is triggered on starting the sweep.

Sig. gen.: 741.4MHz Level	Action	Logic level at X140.C20	Logic level at X140.C21
- 20 dBm	Interrupt Reset	High	High
- 13 dBm	Interrupt Reset	High	Low
- 2 dBm	Interrupt Reset	Low	Low

7.4.2.4 Noise Figure

Test setup

Terminate X152 with 50 Ω.

Measurement

Settings on FSE:	Center	120 MHz
	RF ATT	0 dB
	RBW	2 kHz
	Ref. Level	-40 dBm

- Measure noise with noise marker: < -160 dBm/Hz

7.4.2.5 Intercept (IP3)

Test setup

- Connect two signal generators to X152 via a 3-dB coupler.
- Connect spectrum analyzer with X 158.

Measurement

Settings:	Generator 1	Frequency	741.4 MHz
		Level	- 10 dBm
	Generator 2	Frequency	741.6 MHz
		Level	- 10 dBm
	FSE	Center	120 MHz

- The intermodulation suppression of the test signal should be > 70 dBc.
- Measure the level at X158 at 21.4 MHz and store it as reference level.
- Set generator 1 to 741.5 MHz.
- Measure level at 21.4 MHz.

Spacing to reference value >50 dB

7.5 External Interfaces

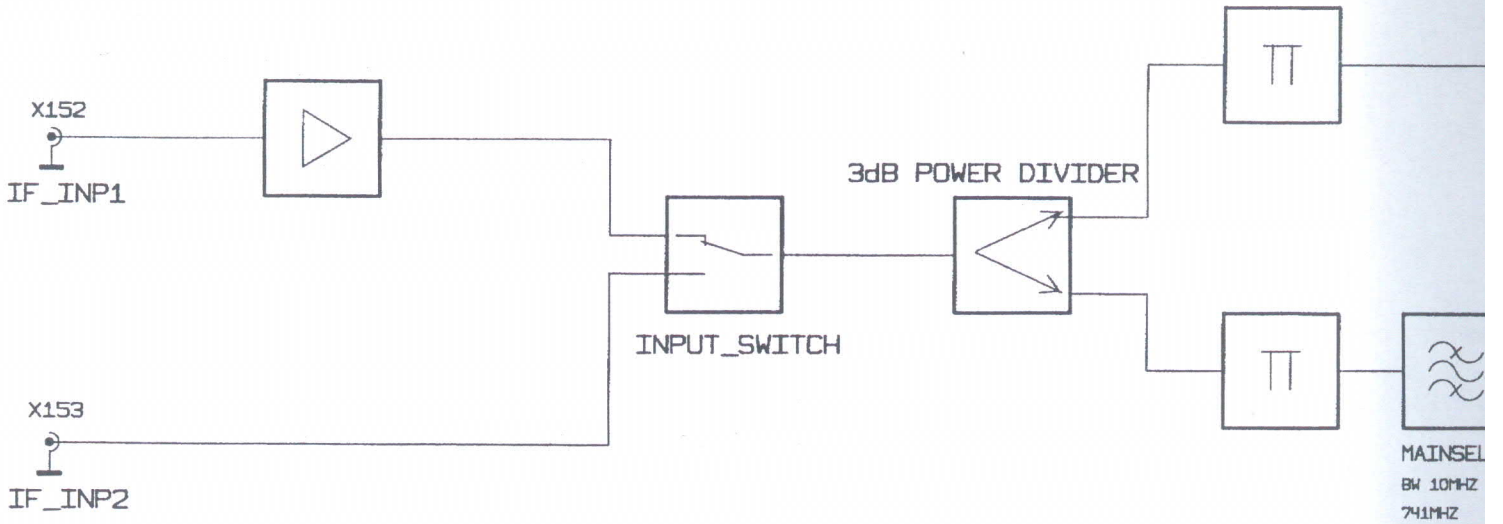
Pin	Name	Input/ Output	From/to	Value range	Signal description
A1	READY	I	FRAC SYN	TTL	Low when latches valid
A10	FTP_CLK	O	FRAC SYN	TTL	Interface to frequency transputer clock
C10	FTP_DAT	O	FRAC SYN	TTL	Interface to frequency transputer data
A11	FTP_STRA	O	FRAC SYN	TTL	Interface to frequency transputer address strobe
C11	FTP_DATR	I	FRAC SYN	TTL	Interface to frequency transputer data
A12	FTP_CLKR	I	FRAC SYN	TTL	Interface to frequency transputer clock
C12	FTP_STRD	I	FRAC SYN	TTL	Interface to frequency transputer address strobe
C17	IF_WIDE	I	IF FILTER	TTL	IF bandwidth 10 MHz
C19	TV_SYNC	O	DETECTOR	1 V_{SS}	TV signal for detector
C20	RF_OVR	O	DETECTOR	open collector	RF overload
C21	RF_OVR-10	O	DETECTOR	open collector	RF overload - 10 dB
A22	LO_unlock	O	DETECTOR	open collector	Synthesizer out of lock
A23	LO_level	O	DETECTOR	open collector	LO level insufficient
A24	INTRES	O	DETECTOR	TTL	Reset of error message
A25	ADCMUX	O	DETECTOR	-5 V to +5 V	Test channel
C26	FTP_SDA	I	FRAC SYN	TTL, 100 kHz	I^2C bus, data
C27	FTP_SCL	I	FRAC SYN	TTL, 100 kHz	I^2C bus, clock
A29	-15V	I		-15 V ± 0.1 V	Voltage supply
C29	-15V	I		-15 V ± 0.1 V	Voltage supply
A30	+15V	I		+15 V ± 0.1 V	Voltage supply
C30	+15V	I		+15 V ± 0.1 V	Voltage supply

Pin	Name	Input/ output	From/to	Value range	Signal description
A31	+5V_A	I		+5.5 V ± 0.05 V	Voltage supply
C31	+5V_A	I		+5.5 V ± 0.05 V	Voltage supply
A32	GNDA	B		0 V	Ground, analog
C32	GNDA	B		0 V	Ground, analog
X151	2ndLO	O	RF MODULE	3.6 GHz, >18 dBm	2nd LO output
X152	IF_INP1	I	RF MODULE	741.4 MHz	IF input RF module
X153	IF_INP2	I	MW CONVERTER	741.4 MHz	IF input MW Converter
X154		I	FRAC SYN	120 MHz, 8 dBm	Reference input
X155	720 MHz	O	LOW PHASE NOISE	720 MHz, 8 dBm	720 MHz output
X156	TV-Signal	O		Z = 50Ω; CCVS standard level	TV signal to rear panel, optional
X157	IF_741_OUT	O		741.4 MHz, 500 MHz BW	Panorama output
X158	IF_21.4_OUT	O	IF FILTER	21.4 MHz 5 MHz/10 MHz BW	Bandwidth switchable

ROHDE&SCHWARZ

Stromläufe
Bestückungspläne
Circuit diagrams
Components plans
Schémas de circuit
Plans des composants

(R 29500 Bl 4)
095.1000 Bl. 4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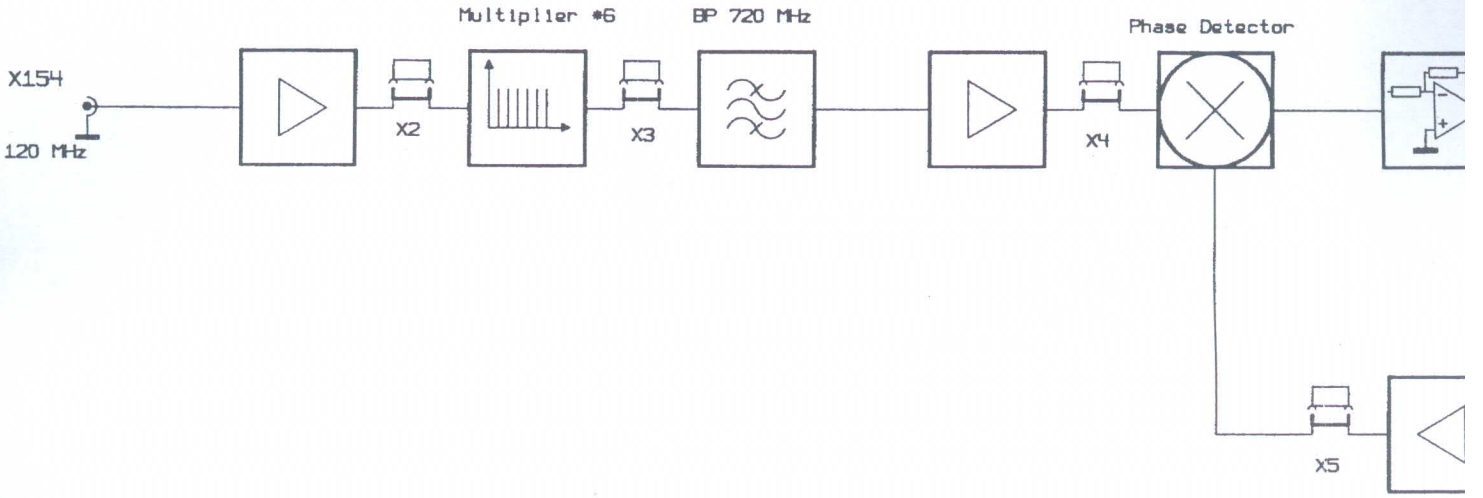
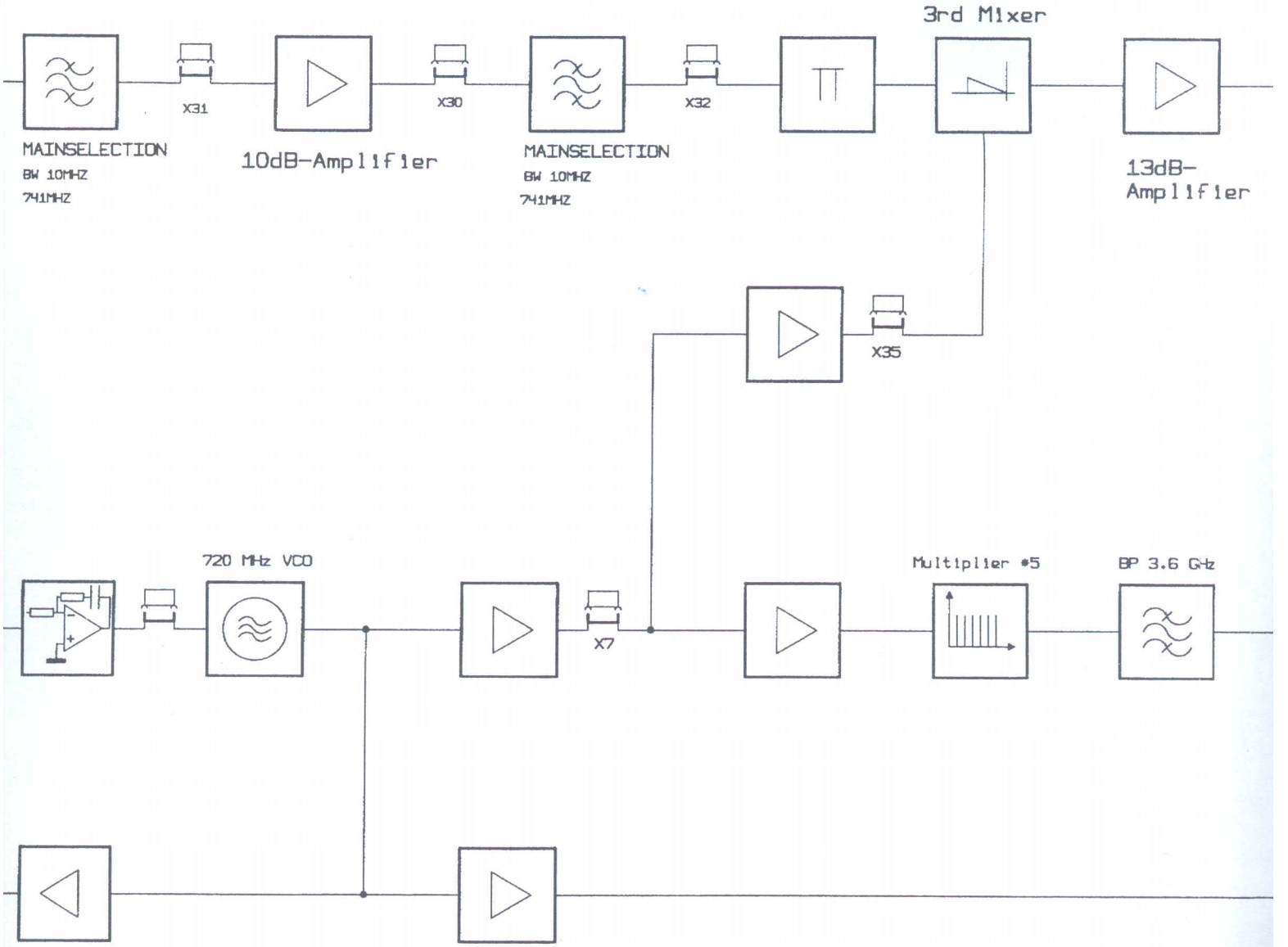
X153
IF_INP2
INPUT_SWITCH
3dB POWER DIVIDER
MAINSEL
BW 10MHZ
741MHZ

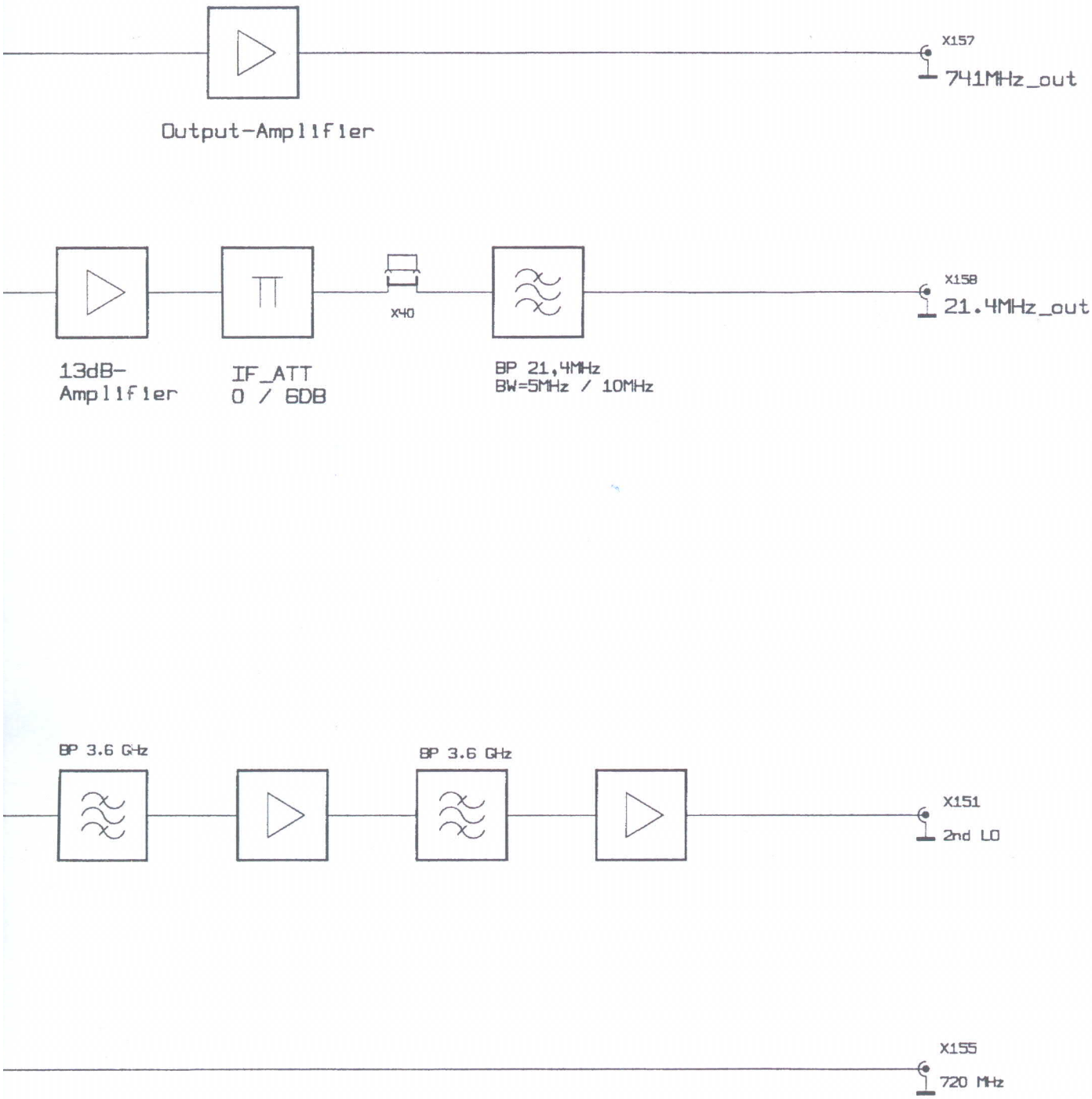

X154
120 MHz
X2
Multiplier *6
X3
BP 720 MHz
X4
Phase Detector
X5

Out



ACHTUNG: EGB!
ELEKTROSTATISCH GEFAEHRDETE BAUELEMENTE ERFORDERN EINE BESONDERE HANDHABUNG.
ATTENTION ESD!
ELECTROSTATIC SENSITIVE DEVICES REQUIRE A SPECIAL HANDLING

03/05	493
03/05	493
AEND. IND.	AEND MITT



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				GEPR.		BERG	
				NORM			
				PLOTT	30.06.95		top sheet1
03/05	49328(43)	11.05.95	NL	ROHDE&SCHWARZ			ZEICHN.-NR. 1065.7012.01S BLATT-NR. 2 v. 10 BL.
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ZU GERAET FSEA			REG.I.V. 1065.6000 ERSTE Z. 1065.6000

ROHDE&SCHWARZ

Service documents

IF FILTER

1065.7264.02

Contents

7 Testing the Module

7.1 Function Description of the Module

7.1.1 Function inside the Instrument

The module processes the 3rd IF of 21.4 MHz from the 2nd IF Converter.

Main functions:

- Resolution filter 1 kHz to 5 MHz
- Switchable IF gain 0 to 50 dB in 0.1-dB steps depending on the reference level and mixer level setting
- Level correction for all bandwidths and frequency response correction with one calibration amplifier each in 0.1-dB steps
- Logarithmic rectifier following the resolution filter for achieving the dynamic display range. Provides the display voltage for the detector.
- Limiting amplifier (included in log rectifier) with TTL output for frequency counter
- AM, FM and quasi-peak demodulator with audio amplifier with input for audio signal from I/Q module

7.1.2 Description of the Block Diagram

The IF FILTER module is controlled by the level transputer.

The IF signal is applied via X168 (50-Ω input) with max. -6 dBm.
It is amplified by 15 dB before reaching the first filter stage.

Resolution filter

The individual models of the FSE family can be delivered with two different versions of the IF filter module. The 20 series (e.g. FSEA20) is equipped with four filter stages, the 30 series with five ones. The resolution filters are synchronously tuned single circuits with buffer amplifiers for attenuation correction. The filters are arranged in two groups with 2 or 3 circuits, with the switchable IF amplifier (Step Gain) and the calibration amplifier connected in-between.
Each filter group consists of two paths, one with LC filters for bandwidths 50 kHz to 5 MHz and one with cystal filters for bandwidths 1 kHz to 30 kHz. For the 10-MHz bandwidth (filters on 2nd IF Converter), the filters are short-circuited.

In the case of the resolution filters, the following parameters are set via D/A converter:

- bandwidth (continuously settable by the transputer; the setting values for the 1,2,3,5 stages are calibrated)

- center frequency (calibrated for all bandwidths)

- positive feedback of the LC filters to compensate for the attenuation of the filters with small bandwidths (only calibration in the factory; the residual error is corrected by the level calibration by means of the calibration amplifier)

IF amplifier

The switchable IF amplifier (STEP GAIN) sets the IF gain of the analyzer. It consists of the Step Coarse and the Step Fine amplifier. The Step Coarse amplifier can be set in 10-dB steps beween 0 and 40 dB. The Step Fine amplifier can be set in 0.1-dB steps between 5 and 15 dB. The gain of the Step Fine amplifier is set via D/A converter. Thus the IF gain can be varied in 0.1-dB steps from 0 to 50 dB (relative).

Switchable attenuator pad
The attenuation of the crystal filters increasing with small bandwidths (1.2 kHz), this gain error is coarsely corrected by switching the attenuator pad ATT1 (exact calibration by means of calibration amplifier).

Calibration amplifier
The CAL AMP1 is set by the frequency transputer by means of D/A converters on the module FRAC SYN. It corrects the RF frequency response of the FSEX. Its gain can be varied in the range -3/+12 dB (relative).
The CAL AMP 2 is set by the D/A converter accommodated on the IF FILTER module. It is controlled by the level transputer. It serves to correct all frequency-independent level errors such as absolute gain of the overall instrument, relative gain error of the bandwidths and the step gain setting. Its gain can be varied in the range -6 to +9 dB (relative).

The characteristics of the calibration amplifiers and the step fine amplifier are stored in 0.1-dB stesp in the EEPROM on the IF FILTER module (only factory-calibration). The characteristics of the amplifiers are temperature-compensated and need therefore not be corrected.

Overload Detector

A fast level dectector with comparator is located at the output of the IF amplifier. Its purpose is to detect overload or underrange (important for autoranging). The test point can also be checked in the self-test.
The overload detector acts on the bus lines IFOVR and IFOVR-10 to the level transputer.

Thresholds:
IFOVR : When the reference level is exceeded by >1.5 dB (typ. 3 dB)
IFOVR-10 : When the reference level is fallen below by > 11 dB (typ. 13 dB)

IF outputs

The module features two outputs where the filtered third IF is applied. The first output X163 leads to the DIGITAL IF module, where the bandwidths 1 Hz (30 Hz in the case of 20 series) to 1 kHz are implemented.
The second output X164 leads to the rear panel, either directly or, if installed, via the option I/Q DEMODULATOR. The output level of a signal at reference level is normally 0 dBm as long as the step gain can be set (mixer level > = -60 dBm). In the case of digital bandwidths ≤1kHz and with vector analysis (I/Q DEMODULATOR) the level is -20 dBm.

Within the module, the IF signal is taken to the demodulator and the log amplifier.

Switchable amplifiers:
For attenuation correction with the 1-kHz bandwidth set, the gain at output X164 both to the demodulator and the logarithmic amplifier is increased by 2 dB.

Level detector:
The transfer level to the log amplifier can be measured in the self-test.
Log amplifier

The logarithmic amplifier consists of three identical integrated limiting amplifiers with logarithmic rectifier characteristic, the video outputs of which are summed up.
Each stage works logarithmically in a 45-dB range. The ranges are joined by operating the first stage via an attenuator pad, the second one via a preamplifier and the third one in cascade with the second stage. The second stage serves as linear preamplifier.
To make sure that the broadband logarithmic amplifier reaches the required dynamic range with smaller resolution bandwidths, switch-selectable noise filters are located ahead of the second and third stage.
The logarithmic amplifier achieves a dynamic range of 110 dB in the case of the 30 series. The 20 series does not feature a third stage, the dynamic range is 90 dB.

Video output:
The IF is removed from the video signal by a lowpass filter. The video signal is taken via X161 to the A/D converter on the DETECTOR where it is also through-connected to the rear panel.

Limiter output:
The logarithmic amplifier also operates as limiting amplifier for the IF signal. A squarewave signal with almost TTL level is taken via X162 to the frequency counter on the DETECTOR module.

Demodulator

The demodulator demodulates the IF signal, providing the AF signal to the loudspeaker or headphones output. The following types of demodulation are possible:

- AM
- broadband FM (FM broadcasting)
- narrowband FM
- QPK (click interference)
- monitoring I/Q demodulator (Option)

The switchover FM broadband/narrowband depends on the IF bandwidth set.
Both with broadband FM and with AM, an AF lowpass filter with a cut-off frequency of 5 kHz is cut in for AF noise suppression.
In EMI receiver mode (Option), the QPK DEMODULATOR is also cut in if the QPK detector is cut in. It improves the audibility of impulse noise, since the AF signal is obtained from the logarithmic video signal.
In Vector Analyzer Mode (Option), the output signal of the I/Q demodulator can also connected to the AF output (via a D/A converter on this module).
The volume of the loudspeaker or headphones output is set via D/A converters at the AF amplifier.

EEPROM

The EEPROM contains all setting values and correction values for the module so that the module can be replaced without adjustment.
As long as the hard disk does not contain current calibration data set, the module is set by means of the EEPROM data.
Every calibration is based on the EEPROM data set.
If the data are totally lost (defective EEPROM), the instrument makes use of a default data set so that the module can at least be operated (without data integrity), e.g. for troubleshooting.

The calibration routines that can be called in the instrument do not allow to determine all data.
In the case of repair inside the module, recalibration might therefore be required using a special test assembly.

Main data:

! Gain correction for the 10-dB steps of the Step Coarse amplifier
! Characteristics for the Step Fine amplifier, CAL AMP1 and CAL AMP2 in 0.1-dB steps
C Absolute gain error with 5-kHz bandwidth
C Relative gain error of the remaining bandwidths
! Center frequency of the individual filter circuits
C Center frequency of the overall filter for each bandwidth
C Setting values for the bandwidths in 1,2,3,5 steps
! Setting value for positive feedback of LC filters
! Video offset voltage of log amplifier
! Temperature coefficients
C Calibration temperature

! cannot be calibrated
C is calibrated

7.2 Measuring Instruments and Auxiliary Equipment

Item	Type of Instrument	Specifications	Appropriate R&S device	Order No.
1	Digital voltmeter	DC 1mV to 15 V	UDS5	349.1510.02
2	Frequency counter	Accuracy $<1 \cdot 10^{-6}$		
3	Signal generator	100 kHz to 3.5 GHz Level 0 to -100 dBm Level linearity at 21.4 MHz: -6 to -46 dBm: <0,1 dB Modulation AM, FM sine, square	SMHU	
4	Signal generator	15 to 30 MHz Level -10 dBm	SMH SMG	
5	Spectrum analyzer	15 to 30 MHz	FSA	
6	Power meter	15 to 30 MHz Linearity 0 to -20 dBm: <0.1 dB	URV5	
7	Network analyzer	15 to 30 MHz		
8	Oscilloscope	100 MHz with 10:1 divider probe		
9	Audio analyzer (distortion meter)	1kHz distortion indication, voltage indication	UPA	
10	3-dB coupler	15 to 30 MHz		
11	Termination	SMB female, 50 Ω ±0.5%		

7.3 Troubleshooting

In the following, a description will be given of how a fault can be clearly located on the IF FILTER module. The module is to be replaced in this case.

Module replacement

- Adjustment of the new module in the instrument is not required.
- **The characteristic of the log amplifier must be calibrated,** since the calibration data are not stored on the IF FILTER module, but in a RAM on the DETECTOR module.
  [→CAL LOG in the CAL menu].
- To ensure data integrity, it is recommended to perform a total calibration which contains the required calibration of the log amplifier [→CAL TOTAL in the CAL menu].
  Besides, it is recommended to carry out a simple function test of the AM and FM demodulator and of the frequency counter using a signal generator.

Important note: Even though the module functions properly again after repair, it can only be used with restrictions.Calibration data that cannot be regenerated may lie out of tolerance so that even calibration does not guarantee data integrity in all cases. This is in particular true for repair work on the STEP GAIN (Step Fine, Step Coarse, CAL AMP1, CAL AMP2) as well as for repair of the individual circuits of the resolution filters. Repair work on the log amplifier and its noise filter may cause a considerable loss of dynamic range.

7.3.1 Self-test

10 self-test voltages can be measured on the module.
Fatal errors such as open circuit in the signal path or total failure of a function can thus be quickly found. Make sure that a 21.4-MHz signal with -6dBm is applied to the IF input (X168). It may also be applied using a signal generator.

Channel	Test signal	Nominal value	Condition
0	LOG_AMP_6VP pos. supply LOGAMP	+6 V ±0.3 V	none
1	LOG_AMP_6VN neg. supply LOGAMP	-6 V ±0.3 V	none
2	VID_OUT Video voltage	+1 V ±0.04 V	ZERO SPAN and signal at reference level
3	reserved		
4	FILT_OUT Level after IF filter	0.8 to 1.6 V typ.1.12 V	ZERO SPAN and signal at reference level
5	STEP_GAIN_LEV Level after STEP GAIN	1.0 to 1.7 V typ. 1.3 V	ZERO SPAN and signal at reference level
6	10V_REF Reference voltage	10 V ±0.28 V	none
7	TEMP Temperature sensor voltage	(0.01·T/°C+2.73) V Indication in °C typ. 45°C (35to55°C)	At an ambient temperature of 20°C, after >30 min. operation
8	reserved		
9	reserved		
10	IF_BW_DAC D/A converter for bandwidth setting	-0.43 [0.37] V ± 30% at 3 MHz -0.84 [0.73] V ±20% at 50 kHz	Values in [brackets] 20 series
11	8_5V Demodulator supply	+8 V ±0.45 V	none
12	ANALOG_GND Analog ground = reference potential	0 ±10 mV	none

The test signals can be individually polled by means of a service function:

X = Channel number

```
SERVICE FUNCTION
    2.26.1.X
```

Notes:
TEST 3: Voltage identical with video signal applied to DETECTOR
TEST 5: Level of IF signal applied to log amplifier.
TEST 6: Level of IF signal at output of IF amplifier (STEP GAIN + CAL AMP's).
TEST 11: The voltage for bandwidth setting may vary after calibration.

7.3.2 Calibration

Total calibration constitutes a comprehensive diagnostic tool [→CAL TOTAL in the CAL menu].
If the error message "Calibration Failed" is output after calibration, the error can be located to a great extent using the calibration result [→CAL RESULTS in CAL submenu].

Below CAL RESULTS, there is a detailed list of the results for each possible RBW referred to bandwidth, center frequency and level (relative). Besides, the result for absolute level and two LOG characteristics for bandwidths 1 to 30 kHz (XTAL) and 50 kHz to 10 MHz (LC) are given.
In the case of bandwidth and center frequency, the deviation from the nominal value and the D/A converter setting value after calibration are indicated. For levels and the LOG characteristic, the deviation from the nominal value before calibration is indicated. In addition, a status message passed, check or failed is output.

Status "check" is no error, but indicates that a relatively large deviation is involved and the adjustment range will soon be exhausted. Module replacement is not required, however, it is recommended in particular if the message "check" already appears at normal ambient temperatures (18 to 28°C).

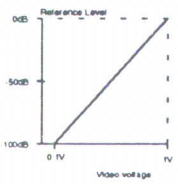
The "check" message appears:
if the bandwidth and center frequency setting for the resolution filters exceeds approx. 80% of the adjustment range,
if the CALAMP 2 (calibration amplifier) features a reserve of less than 1.5 dB,
if the characteristic of the log amplifier deviates from the ideal characteristic by more than ±5 dB.

The message "failed" appears
if a deviation lies outside the adjustment range,
if the characteristic of the log amplifier deviates from the ideal characteristic by more than ±8dB.

7.3.3 Level Error

In the case of smaller level errors, a total calibration should be started first. If the error still occurs then (with or without error message), it can be located according to 7.3.3.1 to 7.3.3.5 depending on the type of error.

If a large level error is involved (>8dB), a calibration does not make sense. In this case, the interfaces IF input and video output on the IF filter should be checked first.



Set Zero Span and check gain from RF input of instrument to IF output of the 2nd IF CONVERTER. Nominal value +4 dB - RF_ATT. If there is no level error yet, use the voltmeter to measure the voltage at the video output of the IF FILTER (X161) with 50 Ω termination.
If an input signal equal to the set reference level is applied, the video voltage must be 1 V. A deviation of 90 mV corresponds to an error of 10dB.

7.3.3.1 RF Frequency Response

If the RF frequency response is too high (deviating level display depending on the RF frequency referred to the display at 120 MHz), there may be an error in the CAL AMP 1.
For checking see 7.4.1. CAL AMP 1. In the case of an error, replace the IF FILTER module.

7.3.3.2 Absolute Level Error (at 120MHz)

Calibrate IF filter [→CAL SHORT in the CAL menu]
a) No error message, but error still present: Check calibration signal, check CAL AMP 2 (see 7.4.1 CAL AMP 2)
b) Error message: IF amplifier or filter faulty, replace the IF FILTER module.

7.3.3.3 Level Error Depending on the Reference Level Set

There might be an error in the STEP GAIN, check as follows:

Set RBW at which the error occurs! Set RF-ATT 0dB. Connect 120-MHz signal generator to RF input. Set level on signal generator and reference level of FSE.
Set reference level -10 dBm to -20 dBm in 2-dB steps, -30 dBm to -60 dBm in 10-dB steps.

The relative level error (reference: display with -10 dBm) with all reference level settings -12 to -60dBm must be <0.2 dB plus the error of the level divider from the signal generator.

In the case of an error replace the IF FILTER module.

7.3.3.4 Level Error Relative to the Reference Level

With constant reference level, the display error depends on the signal level.
There may be an error in the LOG AMP (linearity); check as follows:

Calibrate LOGAMP [→CAL LOG in the CAL menu]
a) Error message: LOGAMP presumably faulty, for checking see 7.4.2.
b) no error message, but error still present: check STEP GAIN according to 7.3.3.3,
or fault in correction RAM → check DETECTOR module.

7.3.3.5 Level Error Depending on Resolution Bandwidth (RBW)

Calibrate IF filter [→CAL RES BW in the CAL menu]
a) Error message (CAL RESULTS Filter Gain): Resolution filter features excessive attenuation for one or several bandwidth settings so that it can no longer be calibrated. Replace the IF FILTER module.
b) no error message, but error still present: CAL AMP 2 does not set the required gain. Replace the IF FILTER module, for checking see 7.4.1 CAL AMP 2.

7.3.4 Error in Frequency Display

(Frequency display after "marker to peak")
At first make sure that the local frequencies are okay:
For this purpose, activate frequency counting (marker count): if the frequency is then indicated correctly, the LOs are correctly set and the IF filter is not centered at 21.4MHz.
Calibrate IF filter [→CAL RES BW in the CAL menu]: in the case of an error message below CAL RESULTS Center Frequency, the filter can no longer be readjusted, replace the IF FILTER module.

7.3.5 Bandwidth Error

Calibrate IF filter [→CAL RES BW in the CAL menu]: in the case of an error message below CAL RESULTS Bandwidth, the filter can no longer be readjusted, replace the IF FILTER module.

7.3.6 Too High Inherent Noise Display

A distinction is to be made between
- absolute level error
- dynamic range of log amplifier
- dynamic range of detector
- noise figure
- discrete interfering signals

Check the level display using a signal generator up to 10 dB abouve noise display. In the case of an error see 7.3.3.

Disconnect IF input from 2nd IF CONVERTER and terminate with 50 Ω.
Check with minimum IF gain (RF-ATT 0dB, Reference Level -10dBm) and small bandwidth (RBW 2 kHz, VBW 100Hz) whether the dynamic range of the log amplifier is sufficient for the noise measurement:
> -80 dB below Reference Level.
In the case of an error additionally check the detector as follows:
Disconnect video output X161: The level display must reach the lower end of the display range (approx. 111 dB below reference level) , otherwise → check DETECTOR module.
Reconnect video output.

Set the bandwidth at which the increased inherent noise is displayed. Display range 100dB, reference level -60dBm, RF-ATT 0dB. Cut in Noise Marker.
If the expected noise figure is exceeded by at least 5dB, the IF FILTER module is okay: → Check RF MODULE and 2nd IF CONVERTER.

If a poor noise figure is obtained, a filter or an amplifier in the IF FILTER is faulty.

An amplifier might be oscillating in the IF FILTER. This may cause the error to occur only sporadically or depending on the temperature.
Connect spectrum analyzer to IF output X163. Check whether interfering signals occur in the range from 100kHz to approx. 200MHz. A considerably increased noise outside the IF bandwidth indicates a tendency towards oscillations. Perform the measurement with various bandwidths: 2kHz, 30kHz, 50kHz, 1MHz, 10MHz.

7.3.7 Too Small Intermodulation Ratio

Check whether there is already intermodulation at the IF output of the 2nd IF CONVERTER or whether it is only produced in the IF FILTER.
For this purpose, check the IF FILTER according to 7.4.8 or check the IF signal as follows:
Set the center frequency at which the error occurs, ZERO SPAN, RF-ATT 0dB.
Using two signal generators, apply a two-tone signal at the RF input via 3-dB coupler (Δf =100 kHz).
Select the level such that each signal is applied to the RF input with -16 dBm.
Using a spectrum analyzer, measure the intermoduation ratio at the IF output of the 2nd IF CONVERTER: It must be ≥60 dB.

7.3.8 Error in Frequency Counting

Select the setting where the error occurs. Connect signal generator to RF input.
Prerequisite: signal >20 dB above noise.

a) No frequency display or display independent of input signal
Select Zero Span, disconnect cable from X162 and check using oscilloscope whether a squarewave signal with at least 1Vpp, frequency 21.4 MHz is applied.
If so, connect frequency counter and check whether the frequency corresponds to exactly 21.4 MHz. Vary the signal generator frequency (max. equal to resolution bandwidth) and check whether the frequency display varies to the same extent.
Error → Limiting amplifier in IF FILTER faulty
Okay → Check DETECTOR module

b) Faulty frequency display
First vary the signal generator frequency within the bandwidth to check whether the frequency display changes accordingly. If no, see below 1.
If the display changes accordingly, the error cannot be on the IF FILTER: → Check reference frequency and synthesizer, check DETECTOR module.

7.3.9 Error in Vector Analysis or with the Digital Bandwidths ≤1kHz

If the error occurs only in conjunction with the I/Q DEMODULATOR (Option) or DIGITAL IF, first check whether the IF FILTER module properly applies the IF signal to these modules.
Connect signal generator to RF input, level = reference-level, select ZERO SPAN and vector analysis or bandwidth <1 kHz. Measure level at X164 or X163. Nominal value -20 dBm ±3 dB.
In the case of an error, the output amplifiers on the IF FILTER are faulty.

7.3.10 Error in Demodulation

No signal at headphones output (or loudspeaker) or heavily distorted signal with AM, FM, I/Q, or volume cannot be set: → Demodulator/ audio amplifier in IF FILTER faulty

If error only occurs in the case of I/Q, check whether audio signal is generated by I/Q DEMODULATOR:
Measure at X160.C19 (IF-FILTER).

7.3.11 Error in IF Overload Display

a) No IF overload display in spite of an overload of more than 6dB
→ Overload detector on IF FILTER faulty

b) IF overload display with level < reference level
Make sure that the overload is not caused by the 1st LO, to this end set start frequency >100 MHz.
Set high IF gain (reference level -50dBm).
If the error still occurs: → Overload detector on IF FILTER faulty
If the error disappears: → Check 2nd IF CONVERTER

c) Permanent IF overload display even without input signal (1st LO not visible either)
IF OVR line is inhibited by a module. The fault can only be located by replacing the module.

7.4 Testing the Specifications

The following describes how to check the module for 100% proper functioning and data integrity without influence of the instrument. In general, this is only required following repair or if an error cannot be found otherwise.
If there is an error in the instrument, proceed according to section 7.3!

The *uncalibrated* characteristics of the IF FILTER module are to be checked:
→ **CAL CORR OFF** in the CAL menu.
The original EEPROM data are used for setting the module and the uncorrected characteristic of the log amplifier is used for the display indication.

All analog data of the module can be checked irrespective of the complete instrument. The instrument only serves for setting the function and the parameters on the module.
In some measurements, the display of the instrument can be used.

7.4.1 Level Measuring Accuracy (IF Amplifier)

Test setup

Signal generator → X 168 (Remove cable to 2nd IF CONVERTER)
Power meter → X163 (remove cable to DIGITAL IF)
Digital voltmeter → X160.A15

Setting on the FSE
Center 120 MHz, ZERO SPAN, RF-ATT 0 dB, Reference Level -10 dBm, RBW 5kHz

Checking the control voltage for CAL AMP1

The control voltage for the CAL AMP1 is derived from the FRACSYN module. First check whether this voltage can be correctly set:
Measure at X160.A15 using voltmeter.

```
X = 4096 (DAC-WERT 0)
X = 8191 (DAC-WERT 4095)
```

SERVICE FUNCTION
2.10.2.6.X

Using the service function, write 0 and 4095 to the D/A converter CAL 1 on the FRACSYN module.
The voltage must be 0±10 mV or +10 V ±100 mV.

Characteristics of the Calibration Amplifiers

Note: Functioning of the calibration amplifiers is a prerequisite for all remaining level accuracies including that of the STEP COARSE amplifier!

Setting on the FSE: Reference Level -20 dBm, RBW = 5 kHz
Setting on the signal generator: 21.4MHz, -30 dBm

CAL AMP1

The measurement can only be performed if the control voltage for the CAL AMP1 is correctly set by the FRACSYN module (see above).

```
X = -3, ... 12 [dB]
```

```
SERVICE FUNCTION
   2.26.20.X
```

CAL AMP1 setting with service function	**Indication of power meter**
0 dB	-14 dBm ±2.5 dB Store indication = REFLEV
-3 dB	REFLEV -3± 0.2 dB
+5 dB	REFLEV +5± 0.2 dB
+12 dB	REFLEV +12± 0.4 dB

Note: Take into account linearity error of power meter!

■ If the control voltage is not set, the CAL AMP1 can only be checked for its functions. To this end, a programmable voltage source is used to apply the voltage from the following table to X160.A15, X160.C16 (ground). Compliance with the characteristic cannot be checked!

set voltage	**Indication of power meter**
1.02 V	-14 dBm ±2.5 dB store indication =REFLEV
0.44 V	REFLEV -3 ±1 dB
2.61 V	REFLEV +5 ±2 dB
7.42 V	REFLEV +12 ±4 dB

```
SERVICE FUNCTION
   2.26.0
```

Reset service function:

The CAL AMP1 must now be in the 0-dB position (because 120 MHz is the reference frequency for the RF frequency response). The voltage must lie between 0.6 and 1.6 V (typ. 1.02 V) depending on the characteristic data for CAL AMP1.

If this voltage is not applied, a voltage of 1 V is to be applied using a voltage source for all subsequent measurements.

CAL AMP2

X = -6, ... 9 [dB]

SERVICE FUNCTION
2.26.21.X

CAL AMP2 setting with service function	Indication of power meter
0 dB	-14 dBm ± 2.5 dB Store indication =REFLEV
-6 dB	REFLEV -6 ±0.2 dB
+5 dB	REFLEV +5 ±0.2 dB
+9 dB	REFLEV +9 ±0.4 dB

Note: Take into account linearity error of power meter!

Reset service function:

SERVICE FUNCTION
2.26.0

Absolute gain error with reference bandwidth and reference level

Setting on signal generator: 21.4 MHz, -6 dBm
Nominal indication of power meter: 0 dBm ±2.5 dB

Relative gain error of STEP GAIN

The high accuracy is required since the STEP GAIN is not calibrated, and serves as reference for the log amplifier characteristic. Take into account the tolerance of the level divider in the signal generator!

STEP COARSE

Reference Level Setting on the FSE	this results in the following STEP COARSE setting	21.4-MHz-signal generator level	Indication of power meter
-10 dBm	0 dB	-6 dBm	0 dBm ±2.5 dB Store indication =REFLEV
-20 dBm	10 dB	-16 dBm	REFLEV ±0.2 dB
-30 dBm	20 dB	-26 dBm	REFLEV ±0.2 dB
-40 dBm	30 dB	-36 dBm	REFLEV ±0.2 dB
-50 dBm	40 dB	-46 dBm	REFLEV ±0.2 dB

STEP FINE

Reference Level Setting on the FSE	results in the following STEP FINE setting	21.4-MHz signal generator level	Indication of power meter
-20 dBm	5 dB	-30 dBm	-14 dBm ±2.5 dB Store indication =REFLEV
-21dBm	6dB	-30dBm	REFLEV +1 ±0.1 dB
-25 dBm	10 dB	-30dBm	REFLEV +5 ±0.15 dB
-29.9 dBm	14.9 dB	-30 dBm	REFLEV +9.9 ±0.2 dB

Note: Take into account linearity error of power meter!

Frequency response of STEP GAIN

Setting on the FSE: RBW = 10 MHz

Reference Level Setting on the FSE	Level of signal generator
-15 dBm	-16 dBm
-25 dBm	-26dBm
-35 dBm	-36 dBm
-45 dBm	-46 dBm
-55 dBm	-56 dBm

With each level setting measure at 21.4 MHz first using power meter and store the measured value. Then set the frequencies 16.4 MHz and 26.4 MHz. Maximum level deviation referred to 21.4 MHz: ±1dB

Relative gain error of bandwidths

As the bandwidth setting is made without filter switching, it is sufficient to measure the maximum and the minimum bandwidth for the LC filters and the crystal filters each.

Setting on the FSE: Reference Level -10 dBm
Setting on the signal generator: 21.4 MHz, -6 dBm

RBW Setting on the FSE	Indication of power meter
5 kHz	0 dBm ±2.5 dB Store indication = REFLEV
1 kHz analog	REFLEV ±2.5 dB
30 kHz	REFLEV ±2.5 dB
50 kHz	REFLEV ±2,5 dB
3 MHz	REFLEV ±2,5 dB
10 MHz	REFLEV ±2,5 dB

Note: The center frequency offset of the filters may pretend a level error. If necessary, vary the frequency of the signal generator in order to find the maximum level. Of course, a network analyzer can also be used.

Testing the second IF output

Setting on the FSE: Reference Level -10 dBm, RBW 5 kHz
Setting on the signal generator: 21.4 MHz, -6dBm
Remove cable from X164

Using the power meter measure the level difference between X164 and X163: <±1.5 dB

7.4.2 Characteristic of Log Amplifier

Note:
The characteristic of the log amplifier can be obtained by reading out the correction data following successful calibration. Measurement of the dynamic range (noise display) see below!

If calibration is no longer possible, or the calibration itself is thought to be faulty, or there are errors in the detector module, the characteristic can be obtained independently as described below.

Test setup

Signal generator → X 168 (Remove cable to 2nd IF CONVERTER)
50Ω termination → X 161 (Remove cable to DETECTOR)
Measure at 50 Ω termination using digital voltmeter.

Setting on the FSE
Center 120 MHz, ZERO SPAN, RF-ATT 0dB, Reference Level -10dBm, RBW 5 kHz

Noise indication

Switch level of signal generator to OFF.

Setting on the FSE	Video voltage	
RBW	20 series	30 series
1 MHz	<240 mV typ. 210 mV	<240 mV typ. 210 mV
5 kHz	<220 mV typ. 190 mV	<55 mV typ. 10 mV

Linearity

Nominal characteristic: Reference point: 820mV Video voltage; slope: -9mV/dB

Set the level of the signal generator such (approx. -26dBm), that the video voltage is exactly 820 mV, store the level = P_{ref}.
Set the level of the signal generator from -101 to -3dBm in 3-dB steps (P_i), measure the video voltage in each case (V_i).

Calculate the linearity deviation: error [dB] = P_i[dBm] - P_{ref}[dBm] - (U_i[mV] - 820) / 9

max. linearity error
20 series ±4 dB (typ.± 2dB) in the range -81 dBm to -6 dBm
30 series ±4 dB (typ. ±1dB) in the range -101 dBm to -3 dBm

Note: Deviations below ±5dB can still be calibrated, however, the module should be replaced if ±4 dB is exceeded.

7.4.3 Limiter Output (→Frequency Counter)

Test setup

Signal generator → X 168 (Remove cable to 2nd IF CONVERTER)
Frequency counter → X162 (Remove cable to DETECTOR)
Additionally measure at X162 using oscilloscope with 10:1 probe

Setting on the FSE
Center 120 MHz, ZERO SPAN, RF-ATT 0 dB, Reference Level -10 dBm, RBW 5 kHz

Frequency of signal generator	Level of signal generator	Indication of frequency counter
21.400 MHz	-6 dBm, -50 dBm, -90 [-75] dBm	21.400 MHz
21.401 MHz	-90 [-75] dBm	21.401 MHz

Values in [brackets] apply to the 20 series

Use an oscilloscope to check whether the voltage at X162 is > 1 V peak-to-peak in the last setting.

7.4.4 Overload and Underrange Detector

Test setup

Signal generator → X 168 (Remove cable to 2nd IF CONVERTER)
Measure at X160.A20 and X160.A21 using digital voltmeter, oscilloscope or logic probe.

Setting on the FSE
Center 120 MHz, ZERO SPAN, RF-ATT 0dB, Reference Level -10 dBm, RBW 5 kHz

21.4-MHz signal generator: Level	Action	Logic level at X160.A20	Logic level at X160.A21
-21 dBm	Interrupt Reset	High	High
-17 dBm	Interrupt Reset	High	Low
-4,5 dBm	Interrupt Reset	High	Low
-1,5 dBm	Interrupt Reset	Low	Low

Interrupt Reset:
Shortly apply X160.A24 to ground or call up service function:

= Interrupt Reset

```
SERVICE FUNCTION
      2.0.1
```

7.4.5 Demodulator

Test setup

Signal generator → X 168 (Remove cable to 2nd IF CONVERTER)
Audio analyzer and oscilloscope → headphones socket
X160.C22 can be measured as an alternative.

Setting on the FSE
Center 120 MHz, ZERO SPAN, RF-ATT 0 dB, Reference Level -10 dBm

AM demodulator

Setting on the signal generator
21.4 MHz, -9 dBm
AM Modulation, fmod = 1 kHz, m = 33 %

Setting on the FSE
RBW 20 kHz
Demodulation AM, Volume 87%

Signal at headphones output
Sine 1kHz, Voltage 0.5 to 1.5V RMS
Distortion factor < 5 %

Set level of signal generator to -69 dBm
Voltage may be reduced by max. 3 dB

Setting on the FSE
Volume 0%
Voltage < 2 mV

FM Demodulator

Broadband FM

Setting on the signal generator
21.4 MHz, -6 dBm
FM modulation, fmod = 1 kHz, deviation = 40 kHz, switch off AM

Setting on the FSE
RBW 200 kHz
Demodulation FM, Volume 87%

Signal at headphones output
Sine 1 kHz, voltage 0.5 to 1.5 V RMS
Distortion factor < 4 %

Set signal generator level to -66 dBm
Voltage may be reduced by max. 3 dB

Narrowband FM

Setting on the signal generator
-6 dBm, deviation= 3 kHz

Setting on the FSE
RBW 20 kHz

Signal at headphones output
Sine 1kHz, voltage 0.5 to 1.5V RMS
distortion factor < 4 %

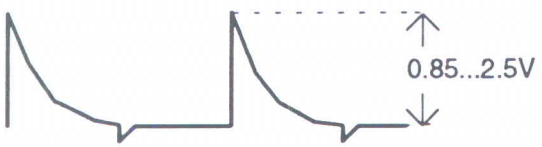
Set signal generator level to -66 dBm
Voltage may be reduced by max. 3 dB

Quasi-peak demodulator
(only with EMI receiver function)

Setting on the signal generator
21.4 MHz, -50 dBm
AM modulation, fmod = 25 Hz square, m = 82 %, switch off FM

Setting on the FSE
EMI Receiver Mode, detector quasi-peak (also cuts in the quasi-peak demodulator)
RBW 120 kHz, Volume (Lautstärke) 87%

The demodulator differentiates the video signal with subsequent pulse expansion and limiting. The purpose is to make clicks audible, to a large extent independently of level and duration.
The signal at the headphones output should be as follows:



7.4.6 Resolution Filters (RBW)

Test setup a) or b)

a) Checking the resolution filters in the properly functioning instrument without measuring instruments:

Setting on the FSE
Select "INPUT CAL" in the service menu
Center frequency 120 MHz, SPAN as indicated below, reference level -40 dBm
The filter parameters can be measured using the marker functions of the FSE.

b) Checking the resolution filters using network analyzer independently of the instrument:

Network analyzer output → X 168 (Remove cable to 2nd IF CONVERTER)
Netzwork analyzer input → X163 (Remove cable to DIGITAL IF)

Setting on the FSE
Center 120 MHz, ZERO SPAN, RF-ATT 0 dB, reference level -10dBm

Setting on the network analyzer
Center frequency 21.4 MHz, output level -10 Bm.
Set the SPAN indicated below on the network analyzer.
The filter parameters can be measured using the marker functions of the network analyzer.

Values in [brackets] apply to the 20 series

Setting on the FSE: RBW 1 kHz analog
Setting on the FSE/NWA: SPAN 15 kHz

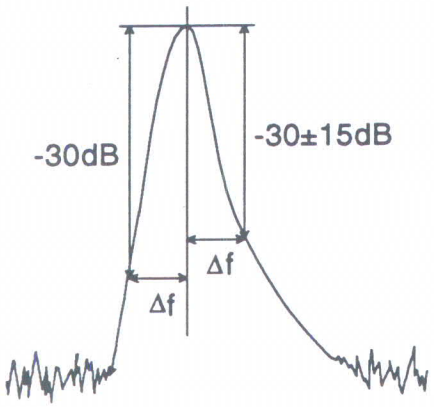
Measurements:
The shape factor 3 dB : 60 dB of the filter is < 1 : 12 [15]
Center frequency error < 500Hz
3 dB bandwidth 700 Hz to 1500 Hz

Setting on the FSE: RBW 30 kHz
Setting on the FSE/NWA: SPAN 500 kHz

Measurements:
The shape factor 3dB : 60dB of the filter is < 1 : 12 [15]
Center frequency error < 60kHz
3 dB bandwidth 15 kHz to 45 kHz

Symmetry

Below the center frequency, a Δf is determined where the attenuation is 30 dB. Δf above the center frequency, the attnuation must be 30± 15 dB.



Setting on the FSE: RBW 50 kHz
Setting on the FSE/NWA: SPAN 750 kHz

Measurements:
The shape factor 3 dB : 60 dB of the filter is < 1 : 12 [15]
Center frequency error < 200 kHz
3 dB bandwidth 25 kHz to 80 kHz

Setting on the FSE: RBW 3 MHz
Setting on the FSE/NWA: SPAN 40 MHz

Measurements:
The shape factor 3 dB : 60 dB of the filter is < 1 : 8 [10]
Center frequency error < 500 kHz
3 dB bandwidth 2 MHz to 4.5 MHz

Check symmetry as with RBW 30 kHz.

7.4.7 Noise Figure

Test setup

50Ω termination → X 168 (Remove cable to 2nd IF CONVERTER)

Setting on the FSE
Center 120 MHz, RF-ATT 0 dB, SPAN = 10·RBW, VBW = 1/10 RBW

Reference Level	RBW	Noise display (noise marker)
-10 dBm	2 kHz	< -143 dBm/Hz *)
	30 kHz	< -151 dBm/Hz *)
	50 kHz	< -139 dBm/Hz
	1 MHz	< -153 dBm/Hz
-40 dBm	2 kHz	< -160 dBm/Hz
	30 kHz	< -158 dBm/Hz
	50 kHz	< -149 dBm/Hz
	1 MHz	< -164 dBm/Hz

*) with the 20 series, measurement is not possible, since indication is limited by log amplifier

7.4.8 Intermodulation (IP3)

Test setup

Two signal generators via 3-dB coupler → X 168 (Remove cable to 2nd IF CONVERTER)
Spectrum analyzer → X163 (Remove cable to DIGITAL IF)

Setting of signal generator
Level -10dBm each, frequencies f1 and f2 see table
(when using a 6 dB coupler -7 dBm)

Make sure that the intermodulation ratio of the test signal is > 80 dBc!

Setting on the FSE
Center 120 MHz, ZERO SPAN , RF-ATT 0 dB, Reference Level -10 dBm

RBW	f1	f2	Measurement using spectrum analyzer
5 kHz	21.4 MHz	21.425 MHz	Measure level at 21.4 MHz, store measured value as reference value.
	21.450 MHz	21.425 MHz	Level at 21.4 MHz must now be at least **68 dB** smaller.
	21.4 MHz	21.401 MHz	Measure level at 21.4 MHz, store measured value as reference value.
	21.402 MHz	21.401 MHz	Level at 21.4 MHz must now be at least **32 dB** smaller.
500 kHz	21.4 MHz	23.9 MHz	Measure level at 21.4 MHz, store measured value as reference value.
	26.4 MHz	23.9 MHz	Level at 21.4 MHz must now be at least **68 dB** smaller.

7.5 Final Testing

Start total calibration [CAL TOTAL in the CAL menu], in the case of "failed" see sect. 7.3.
Check CAL RESULTS for the status "check", in the case of "check" see sect. 7.3.2.

Using a signal generator, perform a simple function test of the AM and FM demodulator (via loudspeaker or headphones) and of the frequency counter (marker count).

7.6 External Interfaces

Signal	D	T	Value range	Terminal	Remark
TEMPFE	A	A	10 mV/K 2.73 V at 0°C	C1	Temperature voltage (Module temp.)
PTP_CLK	E	D	TTL Data rate max. 5 MHz	A7	Interface to level transputer Clock
PTP_DAT	E	D	TTL Data rate max. 5 MHz	C7	Interface to level transputer Data
PTP_STRA	E	D	TTL Data rate max. 5 MHz	A8	Interface to Level transputer Address strobe
PTP_STRD	E	D	TTL Data rate max. 5 MHz	C9	Interface to level transputer Data strobe
CAL_AMP_1	E	A	0 to 10 V Re = 2 kΩ the higher the volt., the higher the gain (~ 0 to 22 dB)	A15	Input for analog CAL amplifier
GNDDAC	E	A	0 V	C16	Reference ground for CAL amplifier input
IF_WIDE	A	D	TTL, static	C17	For controlling the IF filters on the 2nd IF Converter 5/10MHz
I/Q_AF	E	A	± 10 V	C19	AF signal from I/Q demodulator
IF OVR	A	D	TTL open collector LOW = Overload	A20	IF overload
IF OVR-10	A	D	TTL open collector LOW = Overload	A21	IF overload -10 dB (10 dB below IF OVR-threshold)
SPEAKER+	A	A	± 10 V	C22	AF output to loudspeaker
SPEAKER-	A	A	± 10 V	C23	Loudspeaker and AF amplifier ground
INT_RES	E	D	TTL LOW=Reset	A24	Reset for IF OVR and IF OVR-10
PTP_SDA	B	D	TTL 100 kHz	C24	I^2C-BUS, data
ADCMUX	A	A	-5 V to 5 V	A25	Self-test voltage

PTP_SCL	E	D	TTL 100 kHz	C25	I^2C-BUS, clock
+28V	E	V	28 V ± 1V max.10 mA	C28	+28 V supply
-15 V	E	V	-15 V ±0.1 V max. 1.2 A	A29	-15 V supply
-15 V	E	V	-15 V ±0.1 V max. 1.2 A	C29	-15 V supply

Entry in column D (Direction): A = Output, E = Input, B = Bidirectional
Entry in column T (Type) : A = Analog, D = Digital, V = Supply

Signal	D	T	Value range	Terminal	Remark
+15 V	E	V	+15 V ± 0.1 V max. 1,2 A	A30	+15 V supply
+15 V	E	V	+15 V ± 0.1 V max. 1,2 A	C30	+15 V supply
+5 V_A	E	V	5.5 V ± 0.05 V max 100 mA	A31	+5 V supply analog
+5 V_A	E	V	5.5 V ± 0.05 V max 100 mA	C31	+5 V supply analog
GND_A	E	A	0 V ± 10 mV	A32	analog ground
GND_A	E	A	0 V ± 10 mV	C32	analog ground
IF_OUT1	A	A	21.4 MHz, B = RBW Pmax = 0 dBm = REF LEV	X163	IF output to digital IF
IF_OUT2	A	A	21.4 MHz, B=RBW Pmax = 0 dBm = REF LEV	X164	IF output to I/Q or rear panel
LOG_VIDEO_OUT1	A	A	0 to 5 MHz; B = RBW/2; V = 0 - 1 V into 50 Ω	X161	Video output to detector module ADC
LIM_IF_OUT	A	D	21.,4 MHz; B = RBW V = TTL level	X162	limited IF output to detector module PFC
IF_INPUT	E	A	21.4 MHz, Pmax = - 6 dBm = REF LEV	X168	21.4-MHz IF input

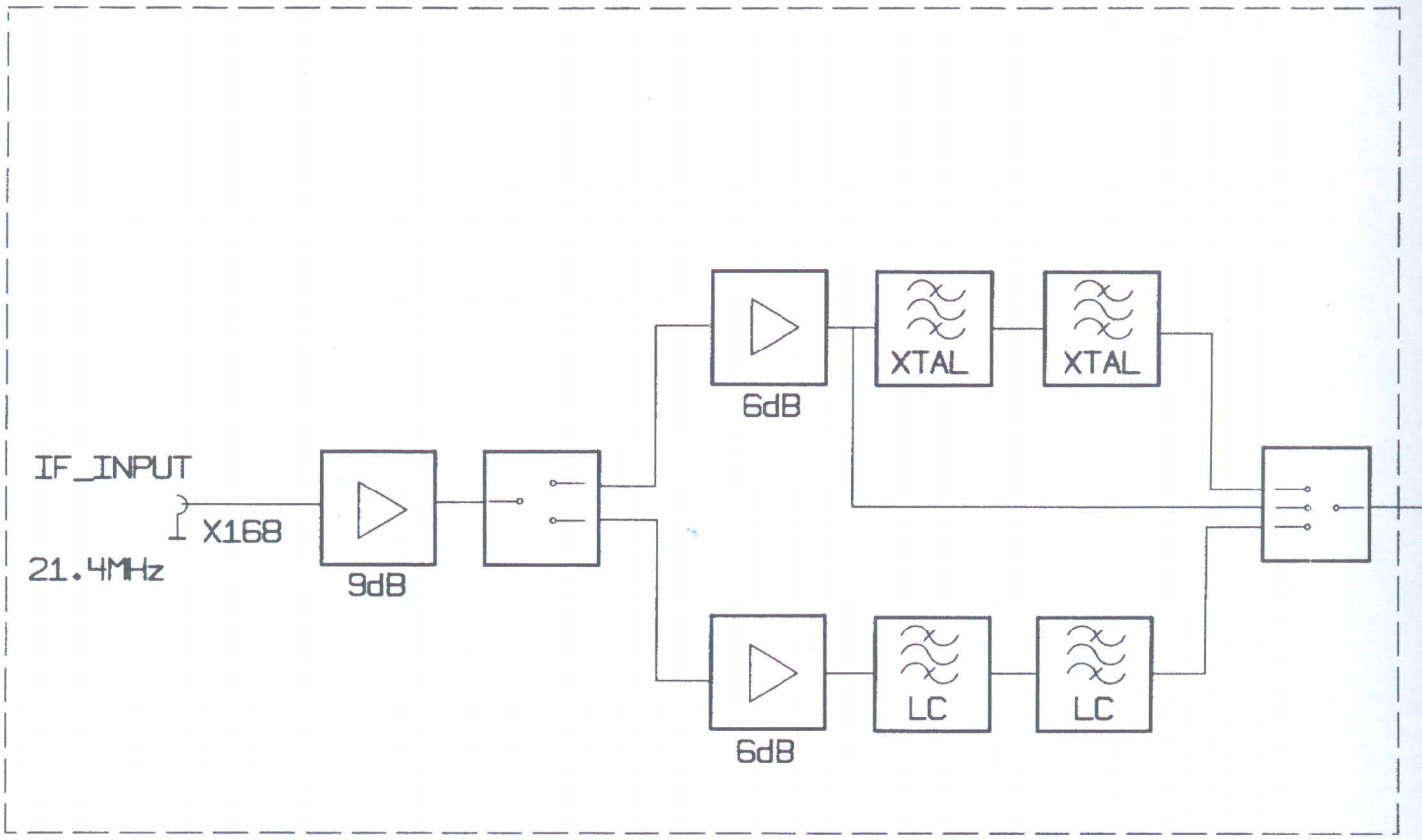
Entry in column D (Direction): A = Output, E = Input, B = Bidirectional
Entry in column T (Type) : A = Analog, D = Digital, V = Supply

ROHDE&SCHWARZ

Stromläufe
Bestückungspläne
Circuit diagrams
Components plans
Schémas de circuit
Plans des composants

(R 29500 Bl 4)
095.1000 Bl. 4

Sheet 16



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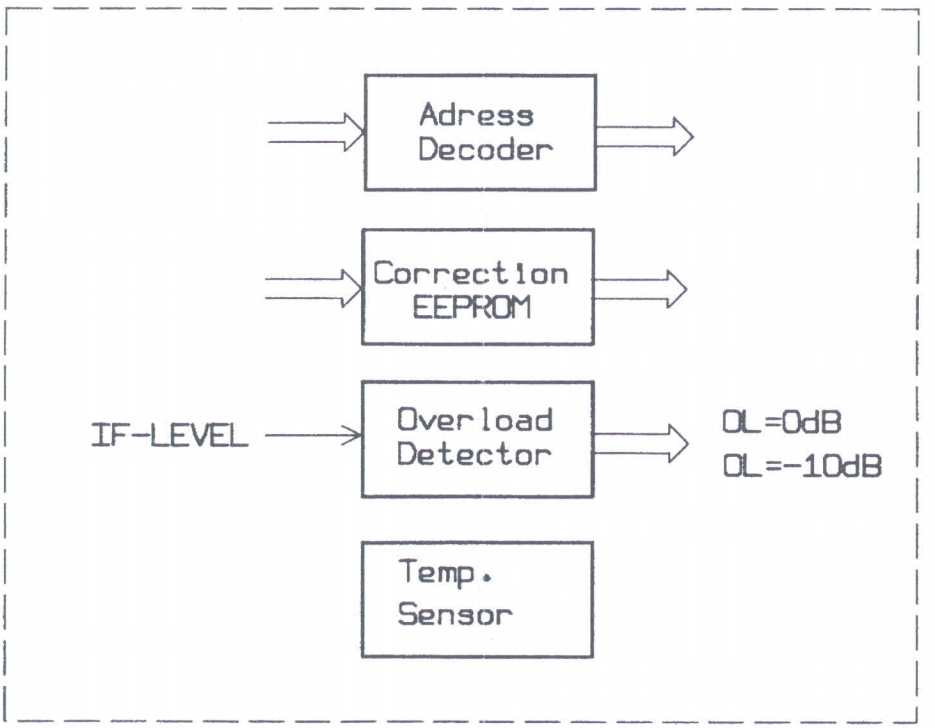

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Sheet 15

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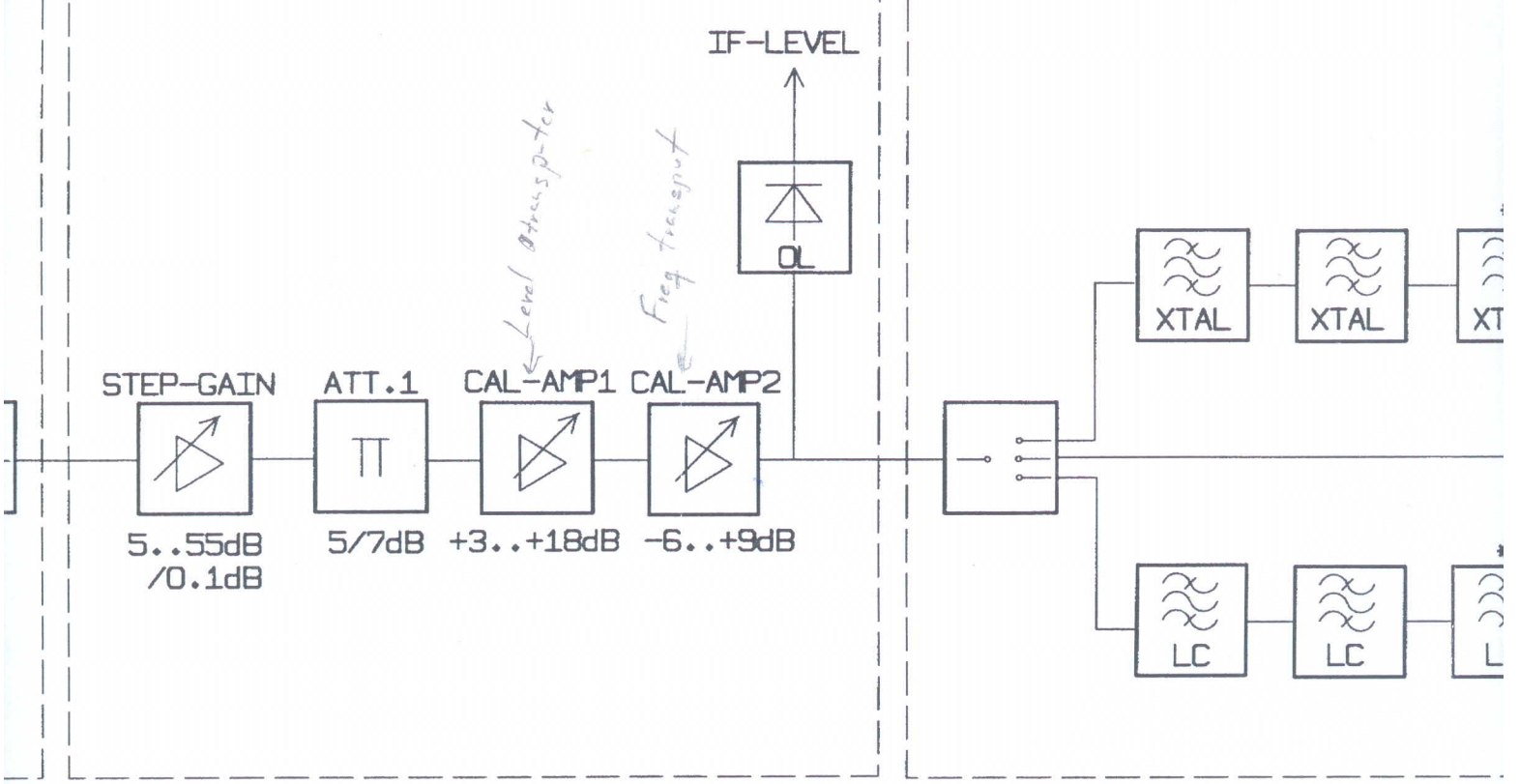

* VAR02 not

Sheet 7 + 8

IF-Filter Control

Sheet 9

Cal-Amp & Step-Gain Control

Sheet 10

Data Latches

Self-Test

05/04	493
05/03	493
AEND. IND.	AEN MIT

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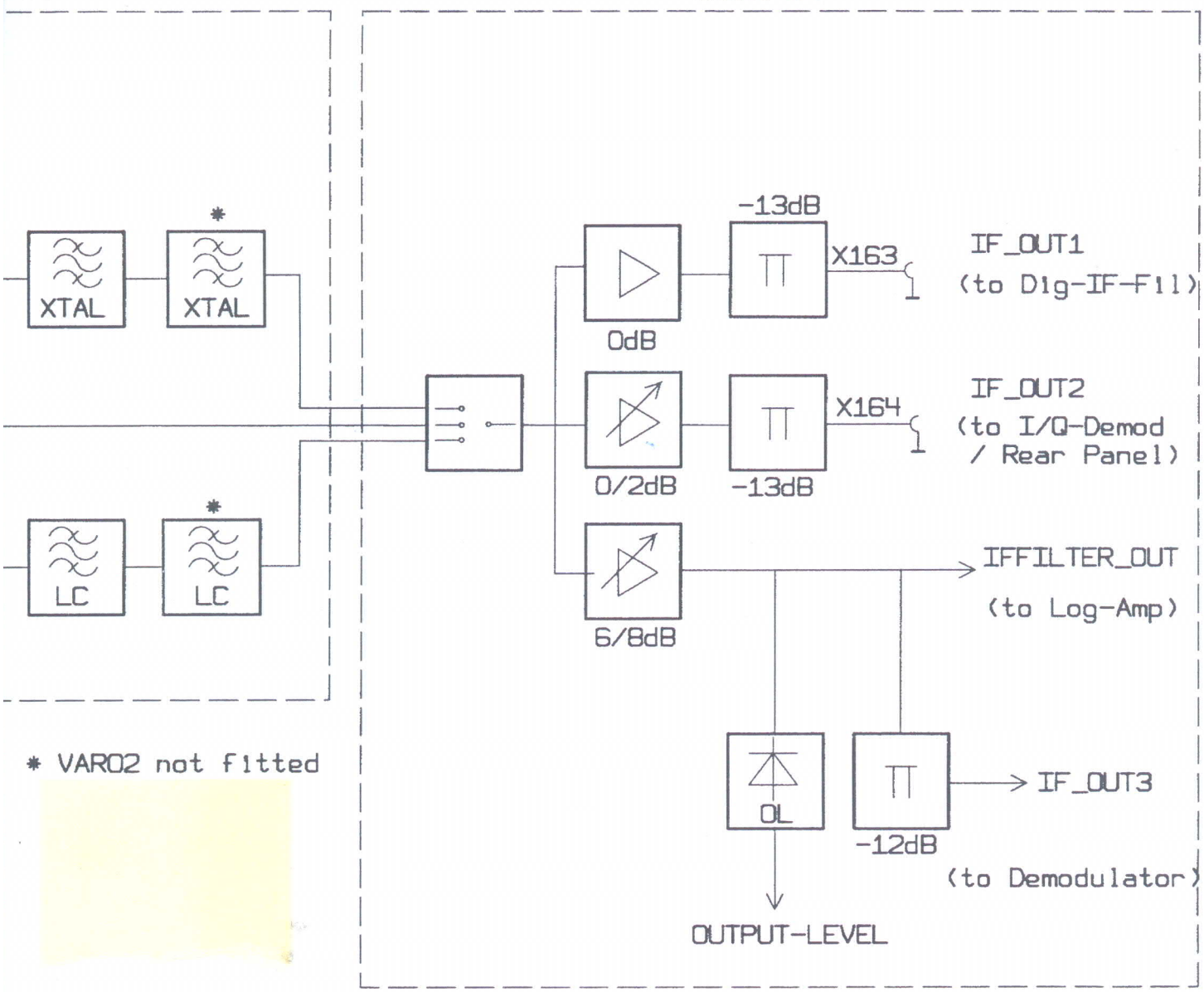

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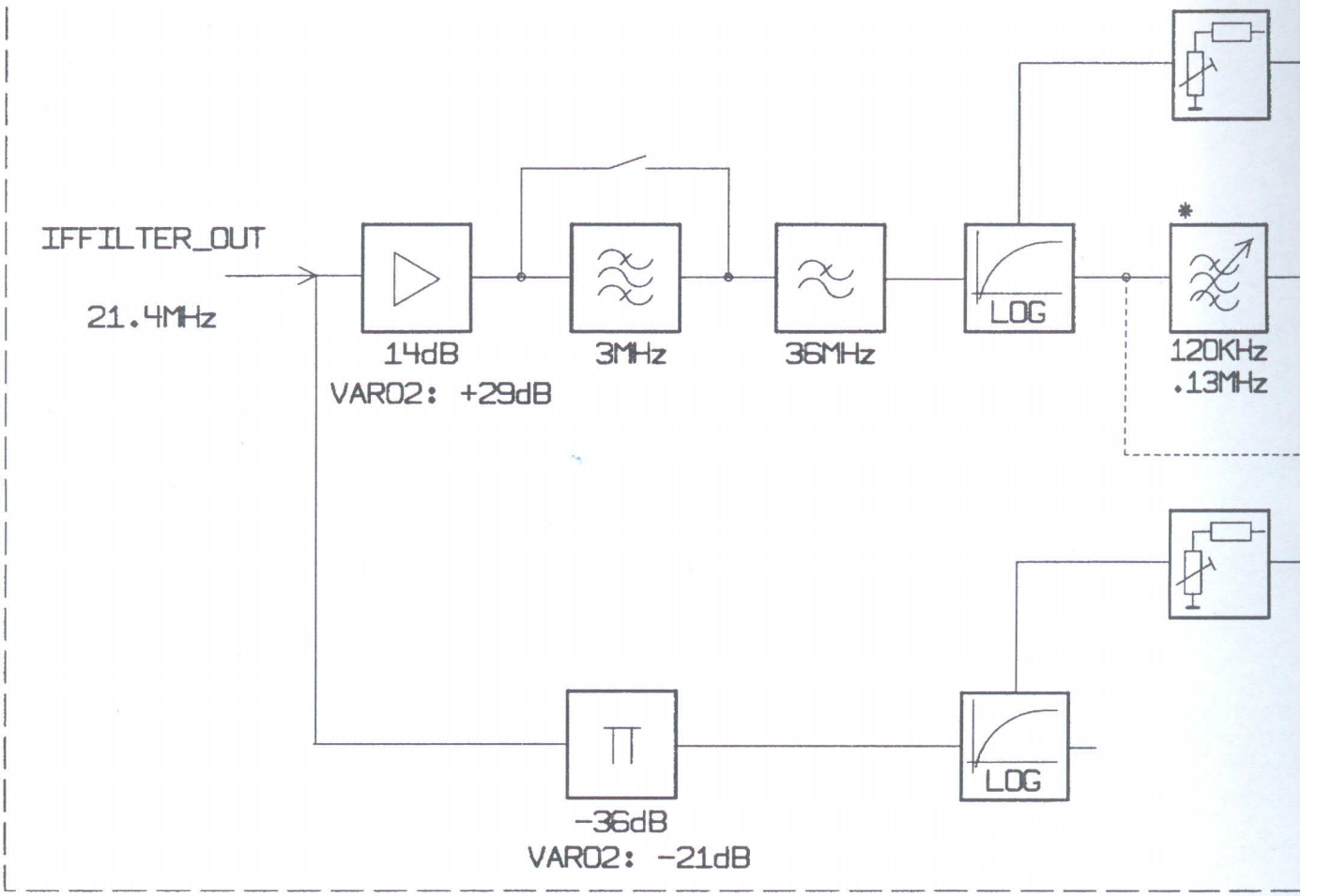
				GEPR.		NL	
				NORM			
				PLOTT	15.09.95		top sheet1
05/03	49328(59)	30.06.95	NL	ROHDE&SCHWARZ			ZEICHN.-NR. 1065.7264.01S BLATT-NR. 2
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ZU GERAET FSE			REG.I.V. 1065.6000 ERSTE Z. 1065.6000 V. 16 BL.

Sheet 11



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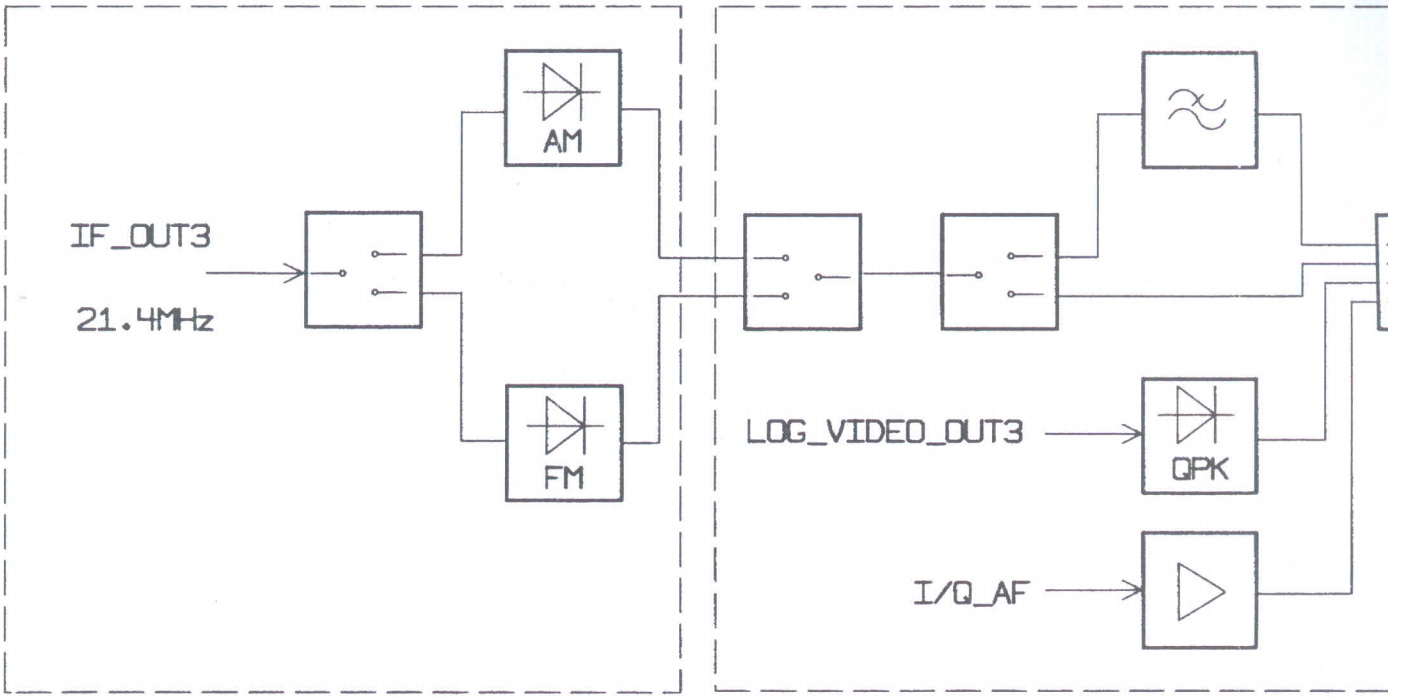

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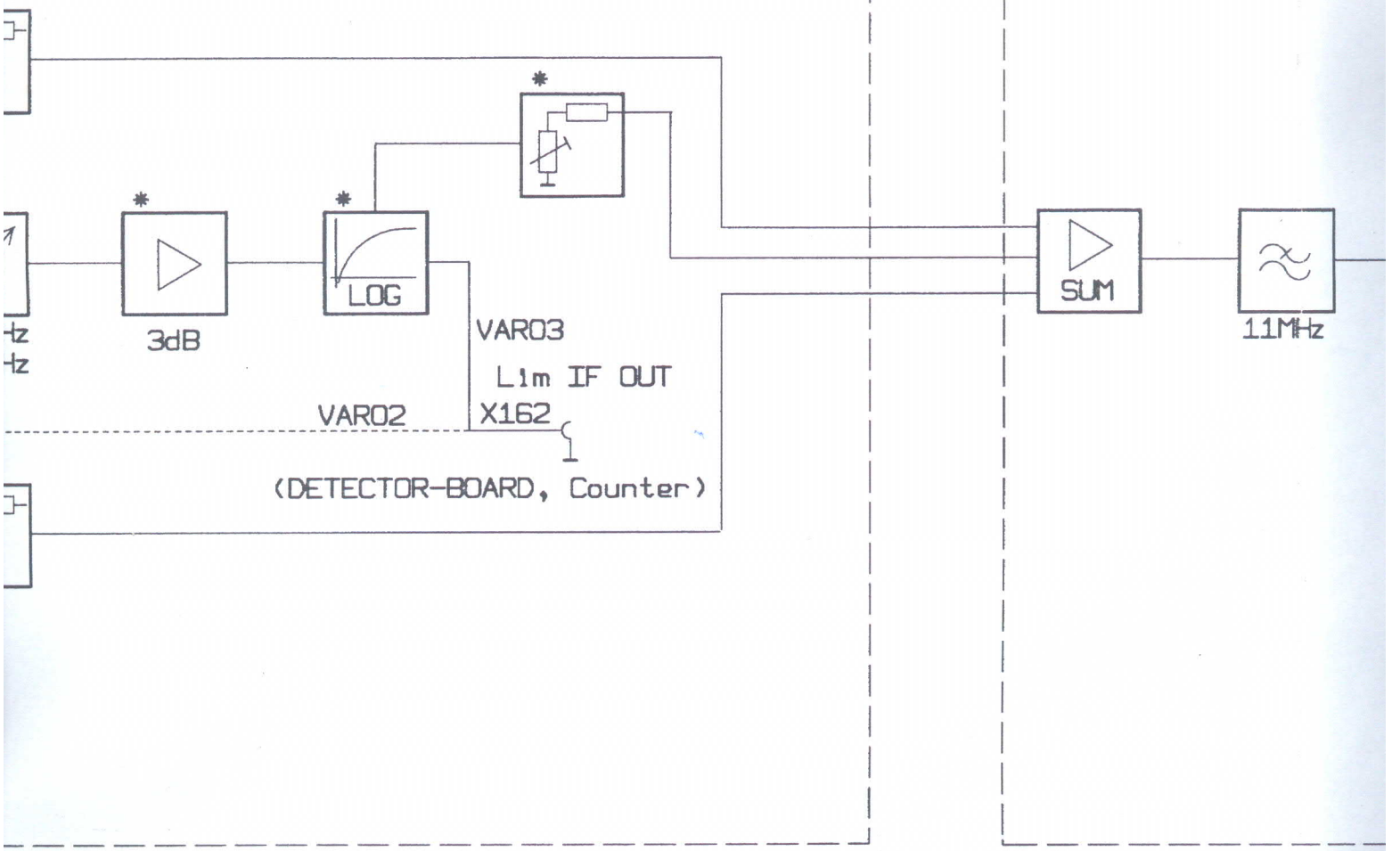

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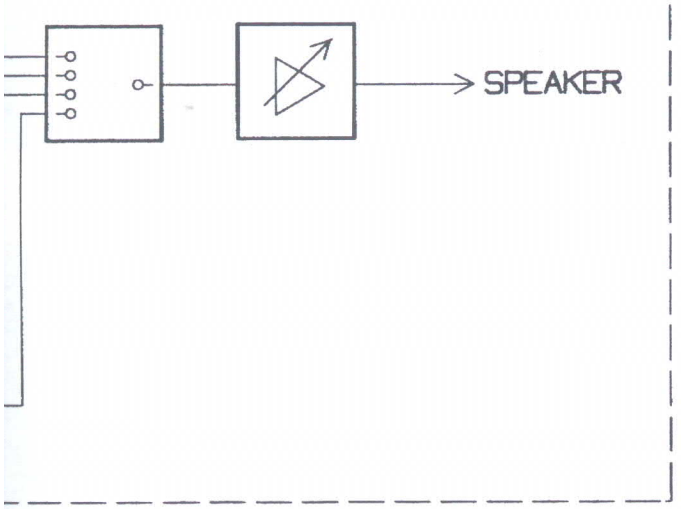

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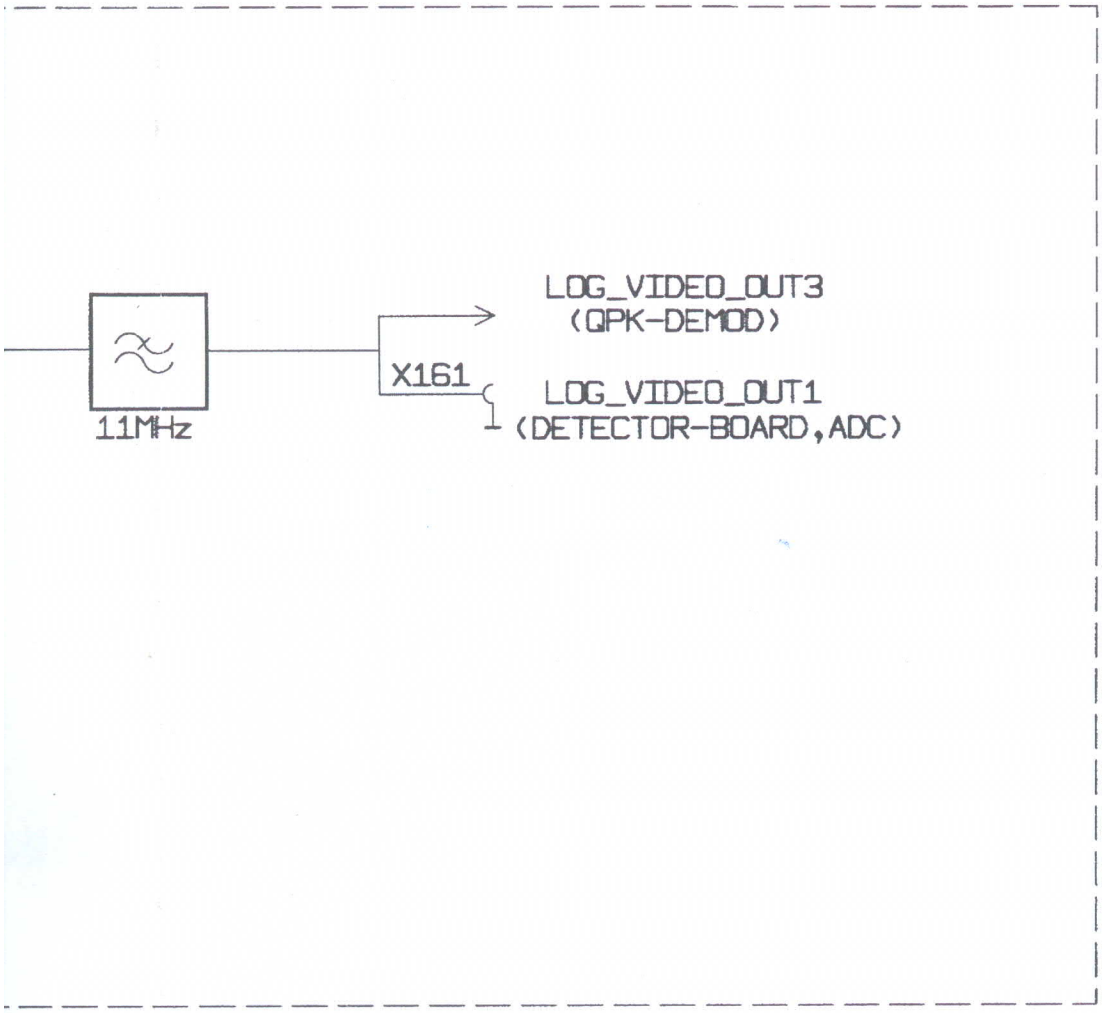

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				NORM			
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				ROHDE&SCHWARZ			ZEICHN.-NR. 1065.7264.01S
05/03	49328(59)	30.06.95	NL				BLATT-NR. 3
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME				V. 16 BL.
				ZU GERAET FSE			REG.I.v. 1065.6000 ERSTE Z. 1065.6000

ROHDE&SCHWARZ

Service documents

DIGITAL IF

1066.0511.02

Contents

7 Testingthe Module

7.1 Function Description of the Module

7.1.1 Function inside the Instrument

The module processes the 3rd Ifof 21.4 MHz from the IF FILTER or the signal from the baseband input (Option).

Main functions:

- Conversion of the 21.4-MHz IF to 25 kHz
- Baseband input DC to 50 kHz (Option)
- Switchable IF gain 0 to 40 dB in 2-dB steps, depending on the reference level and mixer level setting or on the measurement range of the baseband input
- A/D conversion of IF or baseband
- Digital resolution filters 10 Hz to 1 kHz and FFT by means of signal processor

7.1.2 Description of the Block Diagram

The DIGITAL IF module is controlled by the level transputer.

Conversion

The IF signal is applied via X183 (50-Ω input) with max. 0 dBm. It is directly taken to the mixer, where it is converted with the 21.375-MHz LO frequency to 25 kHz. The preamplifier is followed by a switchable amplifier (Step Gain).

Step Gain

Switchable amplifier with 0 to 30 dB in 10-dB steps and additional 0 to 10 dB in 2-dB steps.
The Step Gain processes the 25-kHz IF. With the FFT option built-in, the signal from the baseband input X184 can also be connected to the Step Gain. **Jumper X13 must not be fitted with the option installed.** The switch is located on the option.

Overload Detector

A level detector and a comparator are located at the output of the Step Gain. They permit to detect overloading of the Step Gain and the A/D converter. The test point can also be checked in the self-test. The overload detector acts on the bus line IF_OVR to the level transputer.

Threshold:
Responds when 91% of the measurement range of the A/D converter are exceeded. This corresponds to a level of 8dB above Reference Level.

A/D converter

The IF or baseband signal is taken via an antialiasing filter with a cut-off frequency of 50 kHz to an 18-bit A/D converter. This has a sampling rate of 200kHz, providing a serial data stream to a shift register, which transfers the data to the signal processor in parallel. A sequence control system (EPLD) controls the A/D converter, data transfer to the shift register and to the signal processor.

Signal processor (DSP)

The DSP core is a plug-in module accommodating the signal processor DSP56002 and 8k RAM (20 series) or 32k RAM (30 series). The connection to the serial interface to the level transputer is made via the host interface.

On booting, all applications are loaded into the RAM of the DSP via the host interface.
These are the digital resolution filters (FIR filters) and, in the case of the 30 series, FFT also.
The FFT is also used for signals of the baseband input (option). The absolute-value generation with linear or logarithmic weighting also takes place in the DSP. After interpolation to a sampling rate of 25 kHz, the data are transferred via the serial SSI interface to the DSP of the DETECTOR BOARD.
There, digital video filtering takes places and, subsequently, signal weighting in the detector gate array as in the case of the data from the video A/D converter).

Local Oscillators

The module provides three frequencies:
- Clock frequency for signal processor 20 MHz
- Clock frequency for A/D converter 25.6 MHz
- LO for mixer 21.375 MHz

The 20-MHz reference of the instrument is cut in via the module: input X186 - output X185.
The 25.6 MHz and the 21.375 MHz are derived from a crystal oscillator each, which is synchronized to the 20-MHz reference via a PLL.
When the module is not in operation, the 25.6 MHz and the 21.375 MHz are cut off.

The level of the 21.375-MHz LO is monitored. The detector acts on the bus line LO_LEVEL to the level transputer.
Likewise, locking in of the PLLs is continuously monitored. The error messages act on the bus line LO_UNLOCK to the level transputer.

EEPROM

The EEPROM contains all correction values for the module and, if applicable, for the option, so that module replacement is possible without adjustment.
As long as there is no current calibration data set on the hard disk, the module is set using the EEPROM data.
Each calibration is based on the EEPROM data set.
In the case of a total loss of data (faulty EEPROM), the instrument makes use of a default data set so that operation of the module is possible (without data integrity).

Not all data can be determined by means of the calibration routines to be called up in the instrument. In the case of repair inside the module, recalibration might therefore be required using a special test station.

Main data:

- ! Gain correction for the 2-dB and 10-dB steps of the Step Gain
- C Absolute gain error with 0-dB Step Gain
- ! Gain correction for Step Gain of baseband input (Option)
- ! Absolute gain error of baseband input with 0-dB Step Gain (Option)

- ! cannot be calibrated
- C is calibrated

7.2 Measuring Instruments and Auxiliary Equipment

Item	Type of instrument	Specifications	Appropriate R&S device	Order No.
1	Signal generator	100 kHz to 1 GHz Level 0 to -50 dBm Level linearity at 21.4 MHz: 0 to -20 dBm: <0.1 dB	SMH SMG	
2	Frequency counter	Accuracy $<1 \cdot 10^{-6}$		
3	Power meter	21.4 MHz 0 to -40 dBm	URV5	
4	Oscilloscope	100 MHz with 10:1 divider probe		
5	Termination	SMB female, 50 Ω		

7.3 Troubleshooting

Prerequisite:

The error is assumed to occur only with digital bandwidths ≤1 kHz.

The short calibration for RBW = 2 kHz must be performed with the status "passed" and without "check" in the case of the absolute level error.

In the following, a description will be given of how an error can be clearly located on the DIGITAL IF module. The module is to be replaced then.

Module replacement

- Adjustment of the new module in the instrument is not required.
- In order to ensure proper functioning, it is recommended to perform a short calibration with RBW <1kHz [→CAL SHORT in the CAL menu].
  Besides, with the FFT option installed (baseband input), it is recommended to perform a simple function test of the baseband input in several measurement ranges using an AF generator.

Important note: Even though the module works properly again after repair, it can only be used with restrictions. Calibration data that cannot be regenerated may then be out of tolerance so that data integrity is not even ensured by a calibration. This applies in particular to repair work on the STEP GAIN or A/D converter. The level measuring accuracy can be checked according to section 7.4.3.

7.3.1 Self-test

8 analog self-test voltages can be measured and 8 status bits read on the module. Fatal errors such as open circuit in the signal path or total failure of a component (operating voltage, oscillator) can thus be found quickly.

Make sure that a 21.4-MHz signal with -20 dBm is applied to the IF input (X183). The 20-Mhz system clock TTL signal must be applied to input X186.
The signals can also be applied using a signal generator and a function generator (TTL output).

Channel	Test signal	Nominal value	Condition
0	ANALOG_GND Analog ground = reference potential	0 ±10 mV	none
1	+5VA Reg. Supply A/D converter	+5 V ±0.2 V	none

2	-5VA Reg Supply A/D convertr	-5 V ±0.2 V	none
3	VCXO 21375 Crystal oscillator for LO	+2 to +3.5 V	none
4	VCXO 25600 Crystal oscillator for A/D converter	+2 to +3.5 V	none
5	reserved		
6	Level ADC Input	1.7 V to 2.1 V	ZERO SPAN, RBW <1 kHz and signal at reference level
7	DIGITAL_GND Digital ground	0±200m V	none

The test signals can be individually polled by means of a service function:

X = channel number

SERVICE FUNCTION
2.23.1.X

Status bit	Monitoring function	Meaning	Condition
#0 LSB	Overloading of baseband input [OPTION]	0 = o.k. 1 = overloaded	none
#1	Overloading of A/D converter	0 = o.k. 1 = overloaded	none
#2	PLL for 4th LO (Local Oscillator)	0 = o.k. (locked) 1 = unlocked	System clock 20 MHz at X186
#3	PLL for ADC clock (A/D converter)	0 = o.k. (locked) 1 = unlocked	System clock 20 MHz at X186
#4	Level of 4th LO (Local Oscillator)	0 = o.k. 1 = Level too small	RBW ≤1 kHz cut in
#5	reserved		
#6	reserved		
#7 MSB	reserved		

The status byte can be polled by means of a service function:.

SERVICE FUNCTION
2.23.2

The readout is in the following format:

X MSB	X	X	X	X	X	X	X LSB

In the case of an error-free function, the status byte contains only "0"

0 MSB	0	0	0	0	0	0	0 LSB

7.3.2 Calibration

Only useful in the case of proper functioning of the digital filters and level error.

For the DIGITAL IF module, a short calibration with any bandwidth <1 kHz [→CAL SHORT in the CAL menu] is sufficient. The absolute gain is calibrated.
If the error message "Calibration Failed" appears after calibration, a short calibration with RBW 2 kHz should be performed at any case to exclude that there has already been an error in preceding modules.
The calibration result [→CAL RESULTS in the CAL secondary menu] is given below "Calibration of Digital IF".
The absolute level error before calibration is indicated for the complete instrument in conjunction with the DIGITAL IF module. In addition, a status message passed, check or failed is output.

The status "check" is no error, but indicates that a relatively large deviation is involved and the adjustment range is almost exhausted. The level error is compensated for by the CALAMP2 (calibration amplifier) on the IF FILTER module. The "check" message appears if the reserve of the CALAMP 2 is less than 1.5 dB.

Replacement of the module is not necessary, however, it is recommended in particular if the "check" message already appears at normal ambient temperatures (18 to 28°C).

The message "failed" appears if the deviation lies outside the adjustment range.

7.3.3 No Display or no Resolution Filter can be Detected

a) If, on booting of the instrument, there is an error message saying that the DSP cannot be booted, there is an error in the Host Interface (interface of the DSP to the level transputer), or the DSP receives no reset from the serial interface (serial interface to level transputer), or the DSP receives no clock (20-MHz TTL signal at input X186 present?), or the DSP core itself is faulty. The module is to be replaced then.

b) DSP is successfully booted, however no filter is indicated:

- Noise display (if necessary, set range >100 dB): probably open-circuit in the signal path, see 7.3.4 b).

- no noise display (only horizontal smooth line or no display at all):
No data or no useful data are transferred to the DSP on the DETECTOR BOARD. Error in the SSI interface (DSP) or DSP receives no useful data from A/D converter. The module is to be replaced.

7.3.4 Level Error

a) In the case of smaller level errors, a short calibration with RBW <1 kHz should be started (see 7.3.2). If the error is still there after calibration without error message see 7.3.4.1

b) In the case of a large level error (>8dB), a calibration does not make sense. In this case, the interface IF input should be checked first.

Set Zero Span and RBW <1kHz and check gain from the RF input of the instrument to the IF output of the IF FILTER. (e.g. use signal generator and power meter)
Normal setting: Mixer Level -30dBm, RF-ATT ≥10dB

Reference level	RF-ATT	Gain nominal value RF→ IF (X163 IF-FILTER)
-20 to -30 dBm	10 to 60 dB	0 to -50dB
-20dBm	10 dB	0 dB
-20 to -50 dBm	10dB	0 to +30dB
<-50 dBm	10 dB	30 dB

If there is no level error yet, measure voltage at the ADC input in a self-test.
If a signal equal to the reference level set is applied to the RF input, the test voltage must be 1.7 to 2.1 V (only with Zero Span).
Important: check Step Gain with 0, 10, 20 dB. To this end, set RF-ATT 10 dB, Reference Level 0, -10, -20 dBm.

SERVICE FUNCTION
2.23.1.6

If this voltage is applied, the anti-aliasing filter or the A/D converter is faulty, replace module.

If the voltage is not applied, either an amplifier (Step Gain) or the frequency conversion is faulty. LO level can be checked (in the case of an error, status bit = 1):

SERVICE FUNCTION
2.23.2

X MSB	X	X	**0**	X	X	X	X LSB

Replace module.

7.3.4.1 Level Error Depending on the Set Reference Level

There might be an error in the DIGITAL IF STEP GAIN, or the calibration data are faulty.

Note: The calibration is only made with 0dB STEP GAIN.

Check as follows:
Set RBW ≤1 kHz digital, RF-ATT 10dB. Connect signal generator to RF input. Set same level as reference level of FSE on signal generator.
Set reference level 0dBm, -10 dBm, -20 dBm.

The relative level error (referred to indication with 0dBm) for all reference level settings must be <0.2dB plus error of level divider from signal generator.

In the case of an error replace the IDIGITAL IF.

7.3.4.2 Level Error Relative to Reference Level

With constant reference level, the indication error depends on the signal level.
Error in A/D converter or shift register (e.g. high linearity error or bit error)

Replace DIGITAL IF module.

7.3.5 Too High Inherent Noise Display

A distinction is to be made between
a) absolute level error
b) dynamic range of A/D converter
c) amplifier noise
d) discrete interfering signal

a) Check level display with signal generator up to 10 dB above noise display. In the case of error see 7.3.4.

b) Disconnect IF input from IF FILTER and terminate with 50Ω (X183).
Check whether the dynamic range of the A/D converter is sufficient with 0dB STEP GAIN (RF-ATT 0dB, Reference Level -10 dBm) with the bandwidth RBW 1kHz digital, VBW 10Hz:
Noise display at least 100 dB below reference level (≤-110dBm)

c) Disconnect IF input from IF FILTER and terminate with 50Ω (X183)
Check noise display with 20 dB STEP GAIN (RF-ATT 0dB, reference level -30 dBm) with the bandwidth RBW 1 kHz digital, VBW 10Hz:
Cut in Noise Marker, readout ≤-152 dBm/Hz.

d) An amplifier might oscillate in the DIGTAL IF. This may cause the error to occur only sporadically or depending on the temperature. However, this can only be determined with open module. Use oscilloscope and 10:1 divider to measure at test points X17, X20, X21.

If the noise data are observed, the DIGITAL IF module is okay: → Check RF MODULE , 2nd IF CONVERTER and IF FILTER.

7.3.6 Error in IF Overload Display

a) No IF overload display in spite of overload of more than 8.5dB above reference level

→ Overload detector on DIGITAL IF faulty

Important: This is only true for digital bandwidths ≤1 kHz and Mixer Level ≤-20 dBm, because, with a higher mixer level, the overload display of the IF FILTER is activated first.

b) IF overload display with level < reference level

Make sure that the overload is not caused by the 1st LO, to this end set start frequency >10 kHz.
Set high IF gain (reference level -50 dBm), digital bandwidth ≤1 kHz.
If the error still occurs: → Overload detector on DIGITAL IF faulty
If the error disappears: → check IF FILTER

c) Permanent IF overload display even without input signal (1st LO not visible either)

IF OVR line is inhibited by a module.

Switch off instrument, remove DIGITAL IF module, switch instrument on again.
If the IF overload display has disappeared, the DIGITAL IF module is faulty, otherwise check IF FILTER, 2nd IF CONVERTER.

7.4 Testing the Specifications

In the following, a description is given of how to check the module for functioning and data integrity. In general, this is only required following repair or if an error cannot be found otherwise.
If there is an error in the instrument, proceed according to section 7.3 in any case!

All analog data of the module can be checked irrespective of the corresponding data of the complete instrument. The instrument only serves for setting the function and the parameters on the module and for indicating the digital measured values.
The digital section (A/D converter, DSP with interface) is automatically checked with all functions.

7.4.1 System Clock

The module must receive and pass on the system clock!
This is assumed for all subsequent tests!

Check clock input (X186): 20-MHz TTL signal (coming from FRACSYN module)
Check clock output (X185): 20-MHz TTL signal (must be routed to DETECTOR module)

7.4.2 Internal Clock Generation and Local Oscillator

Setting on the FSE
RBW 100 Hz

There must not be any LO_Level or LO_UNLOCK error message.
Detailed checking is possible by means of the self-test (see 7.3.1).

SERVICE FUNCTION
2.23.2

X MSB	X	X	0	0	0	X	X LSB

7.4.3 Level Measuring Accuracy (IF Amplifier)

Test setup

Signal generator → X 183 (Remove cable to IF FILTER)

Setting on the FSE
Center 120MHz, ZERO SPAN, RF-ATT 0dB, Reference Level -30dBm, RBW 100Hz
Marker

Absolute gain error with reference level

Setting on the signal generator: 21.4 MHz, -20 dBm
Nominal indication of marker: -30 dBm ±2.5 dB

Relative gain error of STEP GAIN

The high accuracy is required because the STEP GAIN is not calibrated. Take into account the tolerance of the level divider in the signal generator!

Reference Level Setting on the FSE (RF ATT = 0dB)	**this results in the following DIGITAL IF STEP GAIN setting**	**Signal generator 21.4MHz level**	**Marker indication**
-30 dBm	20 dB	-20 dBm	-30 dBm ±2,5dB Store indication as reference value (Delta Marker + Reference Fixed)
-20 dBm	10 dB	-10 dBm	Delta = +10 ±0.2 dB
-10 dBm	0 dB	0 dBm	Delta = +20 ±0.2dB

7.4.4 Overload Detector

Test setup

Signal generator → X 183 (Remove cable to IF FILTER)
Use digital voltmeter, oscilloscope or logic probe to measure at X180.A20.

Setting on the FSE
Center 120MHz, ZERO SPAN, RF-ATT 0dB, reference level -30dBm, RBW 1kHz, Marker

Signal generator 21.4MHz Level	Action	Logik level at X180.A20
Starting with -13 dBm, set level such that the marker indication is -23 dBm (7dB above reference level)	Interrupt Reset	High
Increase level such that marker indication is -21.5 dBm (8.5 dB above reference level)	Interrupt Reset	Low

Interrupt Reset:
Shortly connect X160.A24 to ground or call respective service function:

= Interrupt Reset

```
SERVICE FUNCTION
     2.0.1
```

Check by means of selftest: ADC level detector must signal "overload".

```
SERVICE FUNCTION
     2.23.2
```

X MSB	X	X	X	X	X	1	X LSB

7.4.5 PLL Monitoring

Test setup
Use digital voltmeter, oscilloscope or logic probe to measure at X180.A22.

Action	Logic level at X180.A22
Interrupt Reset	High
Remove cable from X186 (system clock) Interrupt Reset	Low

Interrupt Reset:
Shortly connect X160.A24 to ground or call respective service function:

= Interrupt Reset

```
SERVICE FUNCTION
     2.0.1
```

Check by means of selftest: Both PLLs must signal "unlocked".

```
SERVICE FUNCTION
     2.23.2
```

X MSB	X	X	X	1	1	X	X LSB

7.4.6 LO Level Monitoring

Test setup
Use digital voltmeter, oscilloscope or logic probe to measure at X180.A23.

Action	**Logic level at X180.A23**
Set RBW 100 Hz on FSE Interrupt Reset	High
Set RBW 2 kHz on FSE Interrupt Reset	Low

Interrupt Reset:
Shortly connect X160.A24 to ground or call respective service function:

= Interrupt Reset

```
SERVICE FUNCTION
     2.0.1
```

Note: With analog bandwidths, the 4th LO is swutched off.

Check by means of selftest: The LO level monitoring must signal "low level"

```
SERVICE FUNCTION
     2.23.2
```

X MSB	X	X	1	X	X	X	X LSB

7.4.7 Resolution Filters (RBW)

Instead of all digital resolution filters, the 1-kHz filter is to be checked, since this is most influenced by the analog preliminary filter (2 kHz). For this purpose, the instrument must function properly, since testing by means of a network analyzer as with analog filters is not possible.

Setting on the FSE
It is recommended to start CAL RBW (in the CAL menu), since the 2-kHz filter must be calibrated.
Then select "INPUT CAL" in the service menu.
Center Frequency 120 MHz, RBW 1kHz digital (submenu) , SPAN 10 kHz, Reference Level -40dBm
The filter parameters can be measured using the marker functions of the FSE.

The shape factor 3 dB : 60 dB of the filter is < 1 : 6
Center frequency error < 135 Hz
3-dB bandwidth 1 kHz ±100 Hz

7.4.8 Noise Display

Test Setup

50Ω termination → X 183 (Remove cable to IF FILTER)

Setting on the FSE
Center 120 MHz, RF-ATT 0 dB, Reference Level -30 dBm, SPAN = 1 kHz, VBW = 10 Hz,
RBW = 100 Hz

Noise display (noise marker) < -157 dBm/Hz

Note: The noise display is exclusively determined by the A/D converter if the analog section is error-free.

7.5 Final Testing

Set bandwidth ≤1 kHz digital and start short calibration [CAL SHORT in the CAL menu], in the case of "failed" see troubleshooting section 7.3.
Search CAL RESULTS for the status "check", in the case of "check" see section 7.3.2.

If the option FFT input is installed, perform function test with various reference level settings using an AF generator.
For detailed testing of the FFT input see service description of the FFT input option.

7.6 External Interfaces

Signal name	D	T	Value range	Pin	Remark
READY	E	D	TTL	A1	Low = Initialization finished (Power Up)
GND_A	B	V	0 V	A2, B2,C2	Analog ground
GND_A	B	V	0V	A3, B3, C3	Analog ground
GND_D	B	V	0 V	A4, B4, C4	Digital ground
GND_D	B	V	0V	A5, B5, C5	Digital ground
+5V_D	E	V	5.00 to 5.25 V	A6, B6, C6	5 V digital
PTP-CLK	E	D	TTL	A7	Interface to level transputer; clock
PTP-DAT	E	D	TTL	C7	• data
PTP-STR_A	E	D	TTL	A8	• address strobe
PTP-DATR	A	D	TTL	C8	• read data
PTP-CLKR	A	D	TTL	A9	• read clock
PTP-STR_D	E	D	TTL	C9	• data strobe
EXT_DSP0	A	D	TTL	B13	DSP Host Request
DSP0_SC1		D	TTL	B15	Ser. DSP interface SCI
DSP0_SCK	B	D	TTL	B16	Ser. DSP interface SCI
DSP0_SC0		D	TTL	B17	Ser. DSP interface SCI
DSP0_SRD	A	D	TTL	B18	Ser. DSP interface SCI
DSP0_SC2		D	TTL	B19	Ser. DSP interface SCI
IF_OVR	A	D	TTL open collector	A20	Low = IF overloaded, bus line, Here: if the ADC is overloaded

LO_unlock	A	D	TTL open collector	A22	Low = Synthesizer or PLL unlocked, bus line
LO_level	A	D	TTL open collector	A23	Low = LO level too small; bus line

Entry in column D (Direction): A = Output, E = Input, B = Bidirectional
Entry in column T (Type) : A = Analog, D = Digital, V = Supply

Signalname	D	T	Value range	Pin	Remark
INTRES	E	D	TTL, open collektor	A24	Reset line for Interrupt (reset error message)
P_SDA	B	D	TTL 100 kHz	C24	I^2C-bus level transputer
ADCMUX	A	A	-5 to +5V	A25	Meas. channel for self-test
DSP0_STD	E	D	TTL	B25	Ser. DSP interface SCI
P_SCL	E	D	TTL 100 kHz	C25	I^2C-bus level transputer
DSP0_SCLK	B	D	TTL	B26	Ser. DSP interface SSI
DSP0_TXD	E	D	TTL	B27	Ser. DSP interfaceSSI
DSP0_RXD	A	D	TTL	B28	Ser. DSP interface SSI
-15V	E	V	-15 V ± 0.1 V	A29,B29,C29	-15 V operating voltage
+15V	E	V	+15V ± 0.1V	A30,B30,C30	+15V operating voltage
+5V_A	E	V	5.5V ± 0.05V	A31,B31,C31	5 V analog
GND_A	B	V	0V	A32,B32,C32	analog ground
3.IF	E	A	21.4 MHz	X183	IF input, SMB plug
FFT_IN	E	A	DC-50 kHz, ±10 V peak	X184	Baseband input, SMB plug
REF20M_OUT	A	D	20 MHz, TTL	X185	System clock output, SMB plug
REF20M_IN	E	D	20 MHZ, TTL	X186	System clock output, SMB plug

Entry in column D (Dirction): A = Output, E = Input, B = Bidirectional
Entry in column T (Type) : A = Analog, D = Digital, V = Supply

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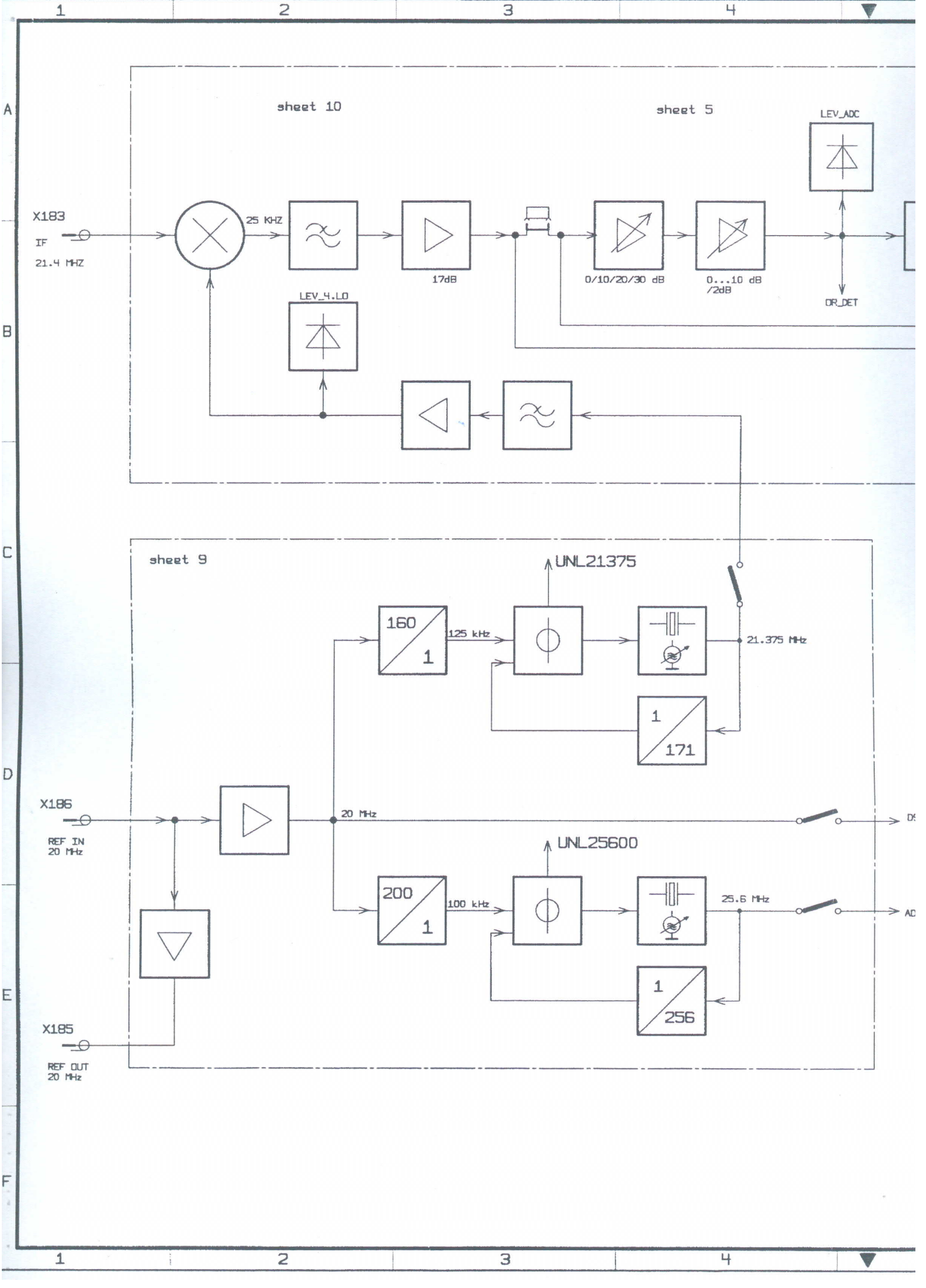
095.1000 Bl. 4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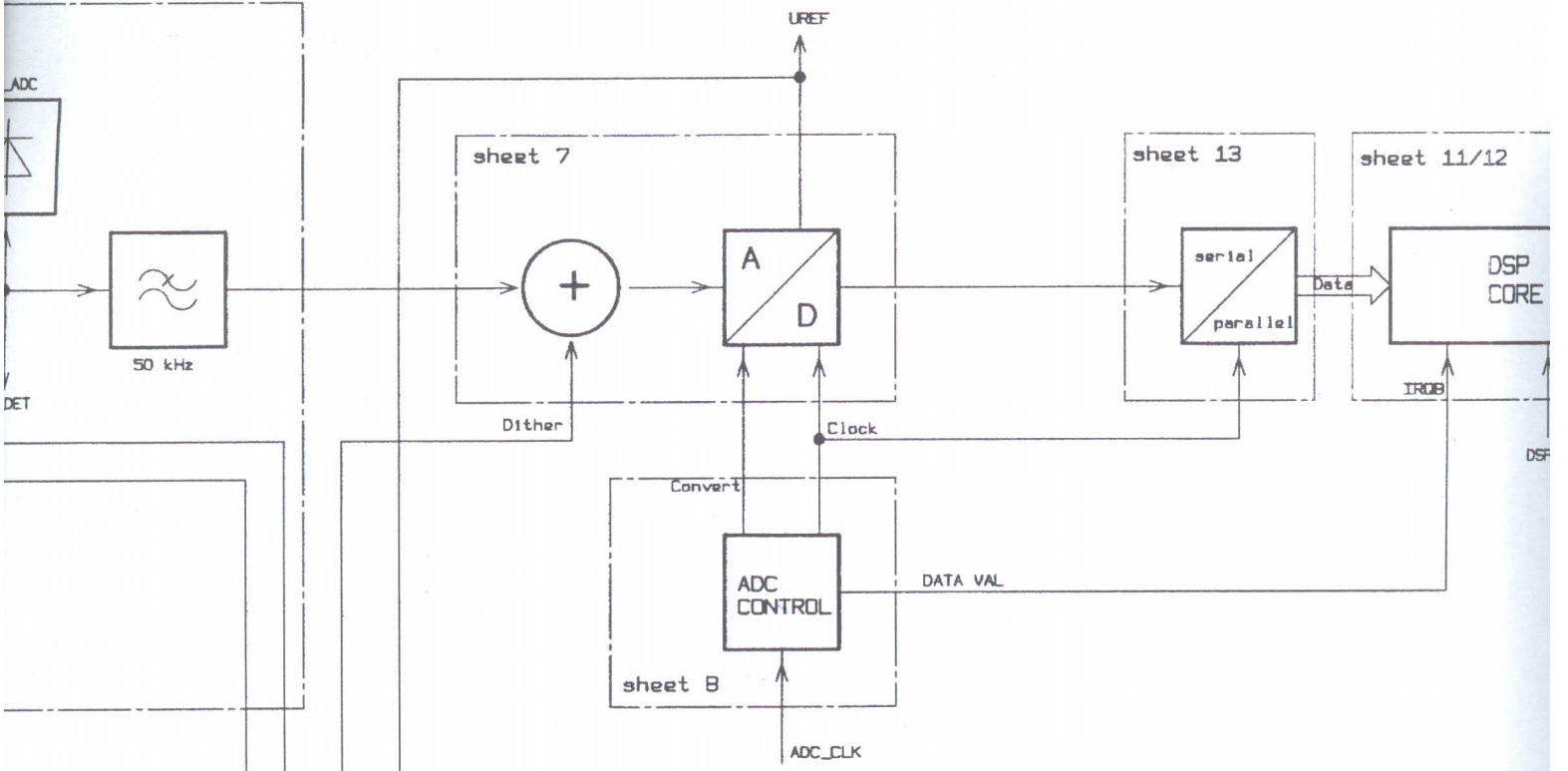
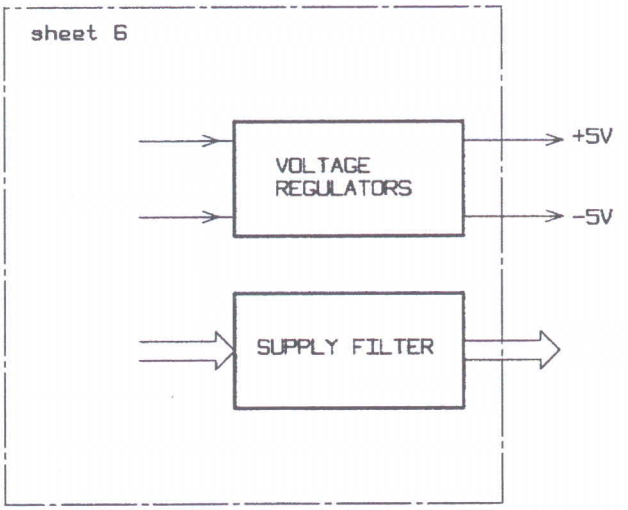
sheet 5
LEV_ADC
X183
IF
21.4 MHZ
25 KHZ
17dB
0/10/20/30 dB
0...10 dB
/2dB
DR_DET
LEV_4.LO
sheet 9
UNL21375
160
1
125 kHz
21.375 MHz
1
171
X186
REF IN
20 MHz
20 MHz
UNL25600
200
1
100 kHz
25.6 MHz
1
256
X185
REF OUT
20 MHz





DSP_CLK

ADC_CLK

FFT_DR

to/from Option
FFT Analysis

VAR 02 = Grundausfuehrung / Basic model

MOD 03 = mit FFT-Analyse / with FFT-Analysis

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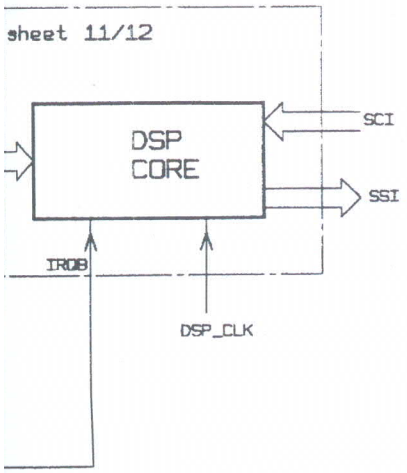

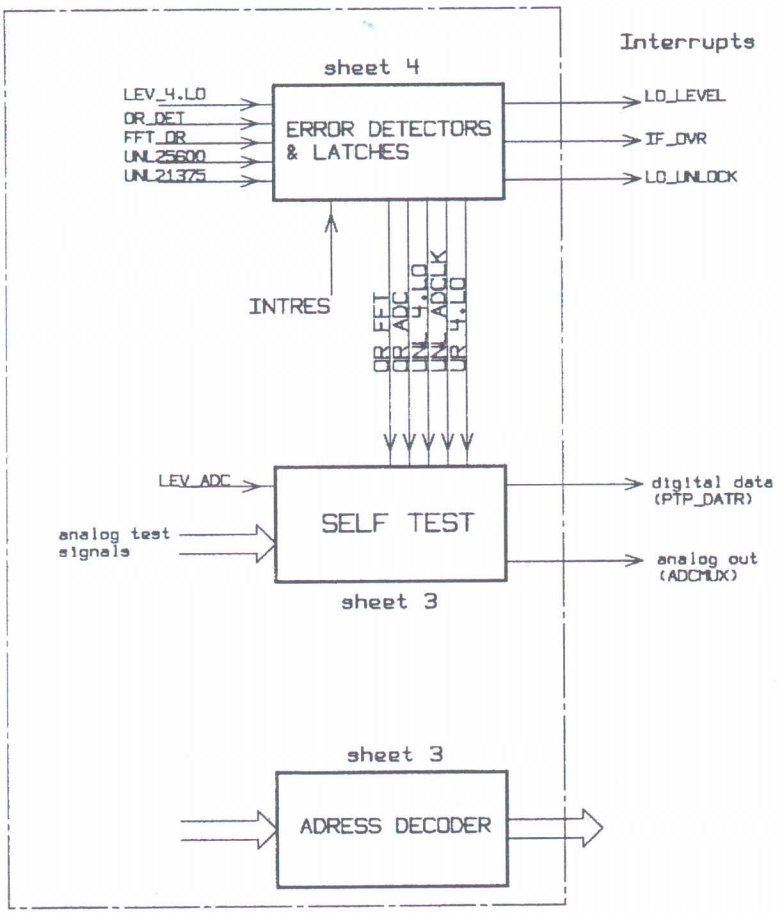

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				NORM				
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				ROHDE&SCHWARZ			ZEICHN.-NR. 1066.0511.01S	BLATT-NR. 1 v. 16 BL.
04/01	49328(31)	5.95	SO					
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ZU GERAET FSEA			REG.I.V. 1065.6000	ERSTE Z. 1065.6000

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ROHDE&SCHWARZ

SERVICE DOCUMENTS
Detektor Board

1065.8019.02

Contents

7 Testing the Module

7.1 Function Description

The Detector Board accommodates the A/D converter for recording analog measured values. The converter is followed by a correction memory, where the characteristic of the log module is linearized. As an option, delogarithmizing for linear display of the measured values can be performed in the correction memory. Video filtering of the corrected measured values is performed in a gate array, which is followed by the digital selection of the detectors (Detector LCA: samples, peak value, average value, RMS). The module also accommodates the triggering of the sweep on internal and external trigger events (trigger LCA). In the case of fast recording of measured values (20 MHz) the values are stored in the measuring RAM (128k*16bit) for later off-line evaluation in the transputer (FAST RAM). The diagnosis/ selftest evaluation for the various analog modules is made by the selftest A/D converter. The analog modules in the signal path are controlled by the serial instrument bus master.

The detector board is used for recording analog measured values, conversion into digital data and their evaluation. The control of the measurement cycles in the spectrum analyzer is derived from this.

The detector board serves the following purposes:

- A/D conversion of the logarithmic IF signal (ADC)
- Linearity correction of the analog log module (and optional delogarithmizing) (COR RAM)
- Video filtering (noise filter gate array and DSP)
- Detection (Detector gate array: Samples, peak value, average value, RMS)
- Triggering on internal and external trigger events (trigger LCA)
- fast recording of measrured values (20 MHz) and storage in the measuing RAM (128k*16bit) for later off-line evaluation in the transputer (FAST RAM)
- Diagnosis/selftest evaluation for various analog modules
- serial instrument bus master for various analog modules

The detector board includes the following plug-in modules:

- **DRAM transputer module** for control of the complex measurement procedures (level transputer).

- **DSP module (DSP_0)** for video filtering with a filter cutoff frequency < 30 kHz and control or data transfer with further DSP modules without direct transputer connection (dig. IF, IQ demodulator)

- a further **optional DSP module (DSP_1)** for **quasi-peak detection** and **IQ demodulation.** From the data stored in the EEPROM or during initialization, the software must determine whether this option is plugged in and take the resulting actions (e.g. initialization, switching the signal paths, events, selftest)

7.2 Measuring Instruments and Auxiliary Equipment

Item	Type of instrument	Specifications	Appropriate R&S device	Order No.	Use
1	Digital multimeter	1 mV to 100 V 0.1 mA to 1 A	UDS5	349.1510.02	
2	Oscilloscope	100 MHz with 10:1 probe divider			
3	Signal generator	21.4 MHz, 0 dBm	SMHU	835.8011	

7.3 Troubleshooting

Using the following description, an error on the DETECTOR board can be clearly located. In the case of an error, the module is to be replaced..

Module replacement

- Adjustment of the module inside the instrument is not necessary.
- The automatic selftest must run without errors after module replacement. A total calibration is to be performed subsequently.

7.3.1 Selftest

Selftest voltages can be measured on the module. These voltages are measued in the automatic selftest with certain instrument settings and checked to determine whether they lie inside a given tolerance window.

Note: *Proper functioning of the modules FRAC SYN, RF Converter, 2nd IF Converter and IF filter and the digital unit. is a prerequisite for running the automatic selftest of the detector board. The automatic testing of the complete instrument is always aborted after the tolerance has been exceeded for the first time to avoid irrelevant error messages. For further fault location also with the aid of externally applied signals, the test functions can be called up manually in the Board Test menu.*

1. **Test GNDA**	Internal test input 2	Nominal value: 0 V	Tolerance:	+/- 10 mV
2. **Test +5VA**	Internal test input 0	Nominal value: +2.75 V	Tolerance	+/- 80 mV
3. **Test -5VA**	Internal test input 1	Nominal value: -2.5 V	Tolerance:	+/- 150 mV
1. **PLL DSP0**	Internal test input 4	Nominal value: > 2.3 V		
2. **PLL DSP1**	Internal test input 5	Nominal value: > 2.3 V	**Perform test only if quasi-peak option or IQ demodulator is installed!**	

7.3.2 Error in the Level Display

If the instrument shows a faulty video signal or none at all on the screen, check the input signal on the detector board:

Instrument settings: Center 120 MHz, Span 0 Hz, Ref.LEV -20d Bm
Apply transmit signal with 120 MHz, -20 dBm

Measurement of input signal at X191: 1V DC

Reduce transmitter level in 10-dB steps down to -100dB, the DC voltage must vary by 90mV with each 10-dB step.

7.3.3 Error in the FREQUENCY COUNTER Function

If the frequency counter displays a faulty value or none at all, first check the 21.4-MH input X194.

Instrument settings: Center 120 MHz, Span 0 Hz, cut in calibration signal
Measurement of input signal at X194: 21.4MHz, TTL level

7.3.4 Error in the Trigger Function

Function LINETRIGGER:

Check input X190 A14: 50-Hz squarewave signal with TTL level

Function RF-TRIGGER:

Instrument settings: Center 120MHz, Span 0Hz, RF-ATT 0dB
Apply transmit signal with 120MHz, 0dBm, 100%AM 1kHz

Check input X190 C11: 1-kHz squarewave signal with TTL level

Function ext. TRIGGER:

Check input X198: Signal from rear-panel socket EXT TRIG GATE

7.3.5 Error when Starting the Module

7.3.5.1 Error in the Transputer Download

If an error occurs during the download, first check the 20-MHz reference input X196, since the clock for the level transputer is derived from this signal. The 20-MHz signal must be immediately available after switching on of the instrument in order for the test program GR_CHECK.EXE (see service documents GRAPHICS) to provide useful results for the two transputers in the analog unit.

7.3.5.2 Error in the LCA Download

If the error message *Download DETECT.BIN Failed* occurs in the DSP download, the file DETECT.BIN on the hard disk should be checked. If no download is possible although the file is correct, there is an error in the detector transputer or LCA.

7.3.5.3 Error in the DSP Download

If the error message *Download BASIS.DLF Failed, Download DSPVIDEO.DLF Failed or Download FIRVIDEO.DLF Failed* occurs during the DSP download, the files on the hard disk should be checked. If no download is possible although the files are correct, there is a fault in the detector DSP.

7.3.5.4 Error in the Serial Interface

If the modules controlled by the level transputer (IF filter, attenuator, digital IF) can no longer be correctly addressed, this may indicate an error in the serial interface. The list Hardware Options in the info menu contains the modules identified by the instrument. If a module is missing, there is probably an error on this module. If all modules or the DETECTOR board are missing, there is a fault on the DETECTOR, or the interface is inhibited by another module. The fault can be further located by withdrawing individual modules.

Note: *The modules FRAC SYN and DETECTOR as well as the connection of the 20-MHz reference must remain inside the instrument!*

7.4 Testing the Specifications

7.4.1 Testing the Signal Path

1. Reference Level 0 dBm with video filter 1MHz

Setting:	Center 120 MHz	Span 0 Hz	Cal source **0 dBm**	Sweep time 20 ms
	Detector to Sample	RBW 1MHz	VBW 1MHz	RF-Atten 0 dB

This results in: **1V DC** at LOG_VIDEO_Input of detector board

Component blocks in signal path:
DC shifter/amplifier of video signal
AD converter
Corr Ram
Noise filter
Detector gate array

Components involved in sequence control: Trigger LCA, transputer module

Nom. result: All 500 measued values must lie within reference level **0dBm** +/- 4 dB.

2. Level -40 dBm with video filter 1MHz

Setting :	Center 120 MHz	Span 0 Hz	Cal-Quelle **-40 dBm**	Sweep time 20 ms
	Detector to Sample	RBW 1 MHz	VBW 1 MHz	RF-Atten 0 dB

This results in: **0.6V DC** at LOG_VIDEO_Input of detector board

Component blocks in signal path:
DC shifter/amplifier of video signal
A/D converter
Corr-Ram
Noise-Filter
Detector Gate Array

Component blocks involved in sequence control: Trigger LCA, transputer module

Nom. result: All 500 measured values must lie within nom. level **-40dBm** +/- 4 dB.

3. Record level -40 dBm with video filter 1MHz in measuring RAM

Setting:	Center 120 MHz	Span 0 Hz	Calsource -40 dBm	Sweep time **100 µs**
	Detector to Sample	RBW 1MHz	VBW 1 MHz	RF-Atten 0 dB

This results in: 0.6V DC at LOG_VIDEO_Input of detector board and recording in measuring RAM

Component blocks in signal path:
DC shifter/amplifier of video signal
A/D converter
Corr-Ram
Noise-Filter
Detector Gate Array
Fast RAM

Component blocks involved in sequence control: Trigger LCA, transputer module

Nom. result: All 500 measured values must lie within nominal level -40dBm +/- 4 dB.

4. Level -40 dBm with video filter 10 KHz

Setting: Center 120 MHz, Span 0 Hz, Cal source -40 dBm, Sweep time **0.1 s**
Detector to Sample, RBW 1MHz, VBW **10 KHz**, RF-Atten 0 dB

This results in: 0.6V DC at LOG_VIDEO_Input of detector board and video filter with DSPA

Component blocks in signal path:
DC shifter/amplifier of video signal
A/D converter
Corr Ram
Noise filter
SP-Module A
Detector gate array

Component blocks involved in sequence control: Trigger LCA
transputer module

Nominal result: All 500 measured values must lie within nominal level -40 dBm +/- 4 dB.

7.4.2 Testing of Detectors

1. **Peak detectors and average-value generation**

Setting: Center 120 MHz, Span 0 Hz, Cal source -40 dBm, Sweep time **20 ms**
Detector to **Auto**, RBW 1MHz, VBW **1 MHz**, RF-Atten **30 dB**

REF-Level -30 dBm
Trace 1 **Max Hold**
Trace 2 **Average**
Trace 3 **Min Hold**

Averaging is to take place over 10 sweeps.

Component blocks involved : Detector Gate Array

Nominal result: The levels of trace 1 (Max Hold) must lie above that of trace 2 (Average Sample), which in turn must lie above that of trace 3 (Min Hold). The interval is about 1 dB in each case, but the important thing is that there are intervals at all.

7.5 External Interfaces

Pin	Name	Input/ Output	Value range	Signal description
B3	DET_DIS	E	TTL	Detector disable
A5,B5,C5	GND_D	B	0V	Ground digital
A6,B6,C6	+5V_D	E	5V +- 0.05 V	5 V digital
A7	PTP-CLK		TTL	Interface to level transputer
B7	LINK_F>P	E	TTL	Link from FTP
C7	PTP-DAT	A	TTL	Interface to level transputer
A8	PTP-STR_A	A	TTL	Interface to level transputer
B8	LINK_P>F	A	TTL	Link to FTP
C8	PTP-DATR		TTL	Interface to level transputer
A9	PTP-CLKR		TTL	Interface to level transputer
B9	LINK_P>G	A	TTL	Link to GTP
C9	PTP-STR_D	A	TTL	Interface to level transputer
A10	TV_SYNC	E	TTL	CVS input
B10	LINK_G>P	E	TTL	Link from GTP
C10	SYNC0	B	TTL	Synchr. with IQ
A11	SYNC1	B	TTL	Synchr. with IQ
B11	LINK_P>F	A	TTL	Link to FTP
C11	SYNC2	B	TTL	Synchr. with IQ
A12	SYNC3	B	TTL	Synchr. mit IQ
B12	LINK_F>P	E	TTL	Link from FTP
C12	Det1	?	TTL	
A13	EXT_DSP_CTRL0	A	TTL	reserved ext DSP Ctrl
B13	LINK_P>A	A	TTL	Link to Adapt.
C13	Det2	?	TTL	
A14	LINE_TRG	E	TTL	Tigger input for LineTrigger from power supply
B14	LINK_A>P	E	TTL	Link from Adapt.

C14	Det3			
A15	DSP0_SC1	A	TTL	reserved (Reset for D IF DSP)
B15	DET_HOLD	E	TTL	Hold measured value
C15	DSP0_STD	A	TTL	SCI interface for DigIF DSP
A16	DSP0_SCK	A	TTL	SCI interface for DigIF DSP
B16	DET_MEM	E	TTL	Read measured value
C16	SWP_END_IQ	E	TTL	Event request from IQ
A17	DSP0_SC0	E	TTL	SCI interface for DigIF DSP
B17	DET_RST	E	TTL	Store meas. value., Detector Reset
C17	DSP0_SCLK	E	TTL	SSI interface for DigIF DSP
A18	DSP0_SRD	E	TTL	SCI interface for DigIF DSP
B18	SWEEP_HOLD\	A	TTL, open collector	Stop sweep
C18	DSP0_TXD	E	TTL	SSI interface for DigIF DSP
A19	DSP0_SC2		TTL	
B19	ERROR1	A	TTL, open collector	
C19	DSP0_RXD	E	TTL	SSI interface for DigIF DSP
A20	IF_OVR		TTL open collector	IF-Overload
C20	RF_OVR		TTL open collector	RF-Overload
A21	IF_OVR-10		TTL open collector	IF-Overload-10dB
B21				
C21	RF_OVR-10		TTL open collector	RF-Overload-10dB
A22	LO_UNLOCK		TTL open collector	Synthesizer unlocked
B22	SWP_LED	A		Sweep-display
A23	LO_LEVEL		TTL open collector	LO level too small
B23	DSP0_STD		TTL	
A24	INTRES	A	TTL	Reset line Error message
B24	ANALYSE	E	TTL	TP analysis flag
C24	P_SDA	B	TTL open collector	I2C data
A25	STEST		-5 to +5 V	Test channel

C25	P_SCL	A	TTL open collector	I2C Clock
A26	TEST_GND		0 V	Reference STEST
A27	SYSRST	E	TTL	Power-on reset
C28	+28V	E	28 V +- 1 V	
A29,B29,C 29	-15VA	E	-15 V +- 0.1 V	
A30,B30,C 30	+15VA	E	+15 V +- 0.1 V	
A31,B31,C 31	+5VA	E	5.5 V +- 0.05 V	
A32,B32,C 32	GNDA	B	0 V	
X191		E	0 to V into 50 Ω	log Video Inp 0 to 1 V into 50 Ω
X192		A	0 to 1 V into 50 Ω	log Video Outp
X194	PFC_INP	E	0 to 1 V	Input for frequency counter
X195	REF_OUT	A	TTL	REF 20 MHz output
X196	REF_20M	E	TTL	REF 20 MHz
X197	REF_IQ	E	TTL	Ref from IQ
X198	EXT_TRG	E	-5 V to +5 V	ext TRG/Gate input

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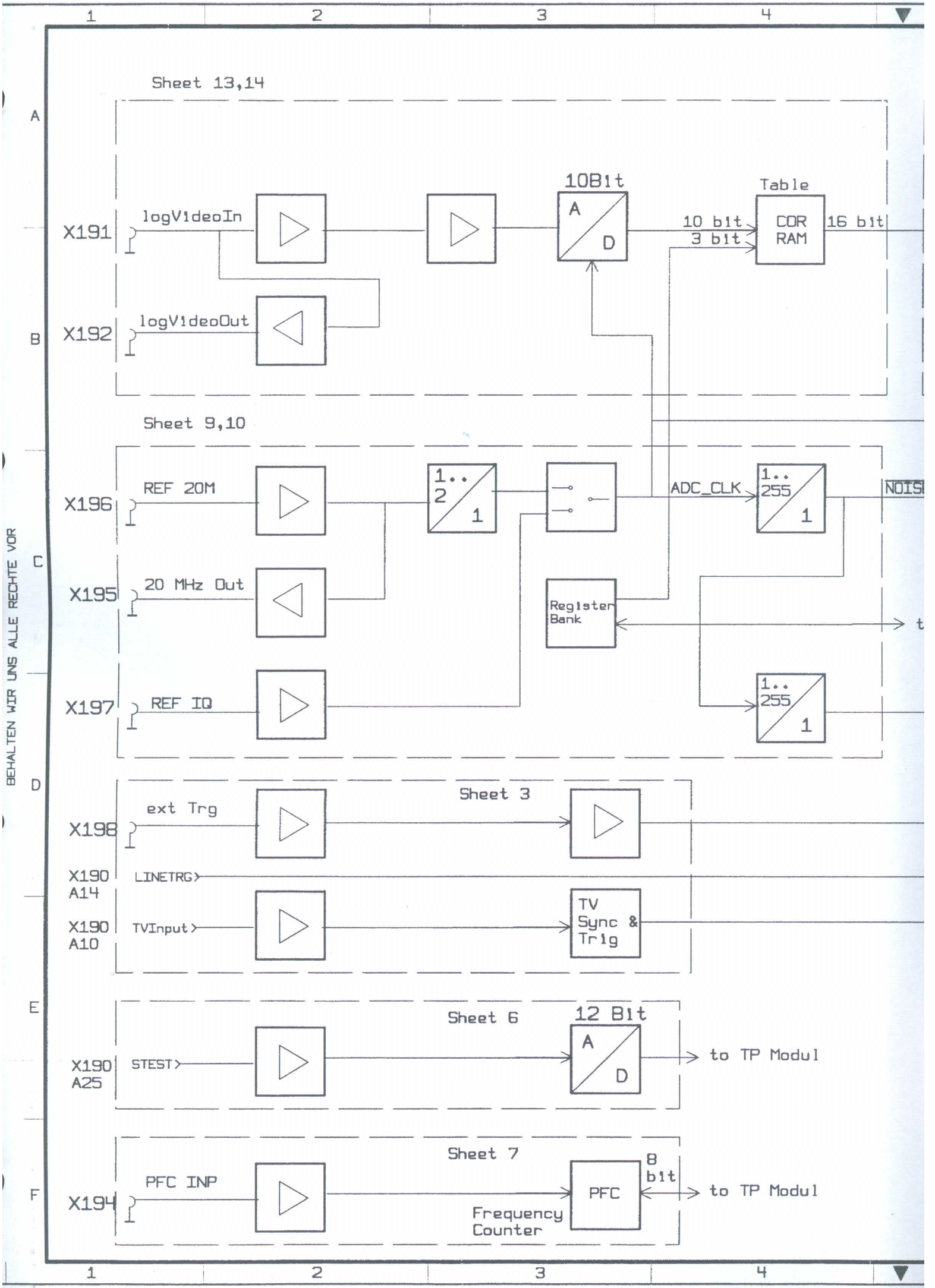
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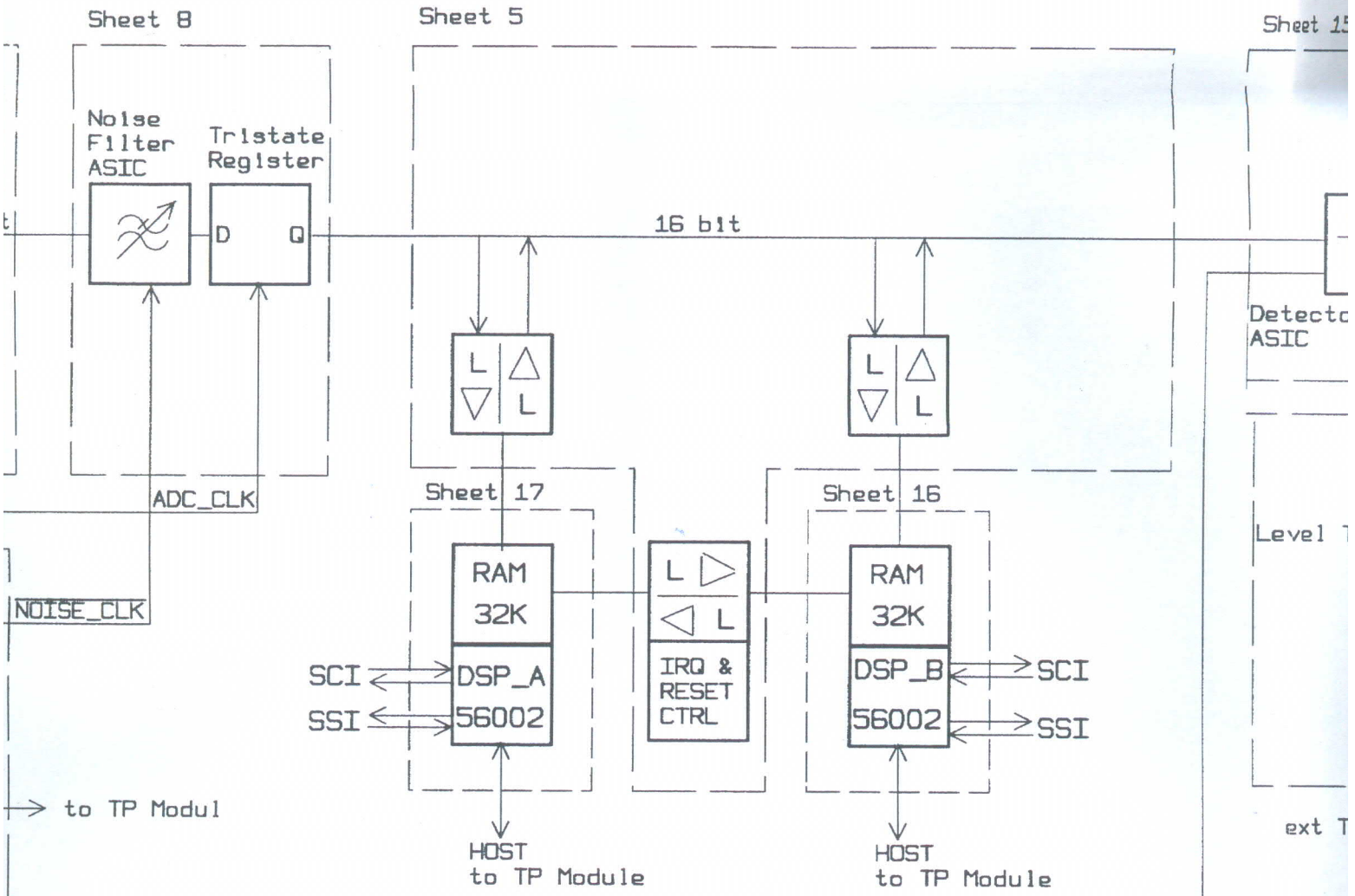
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56002
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32K
DSP_B
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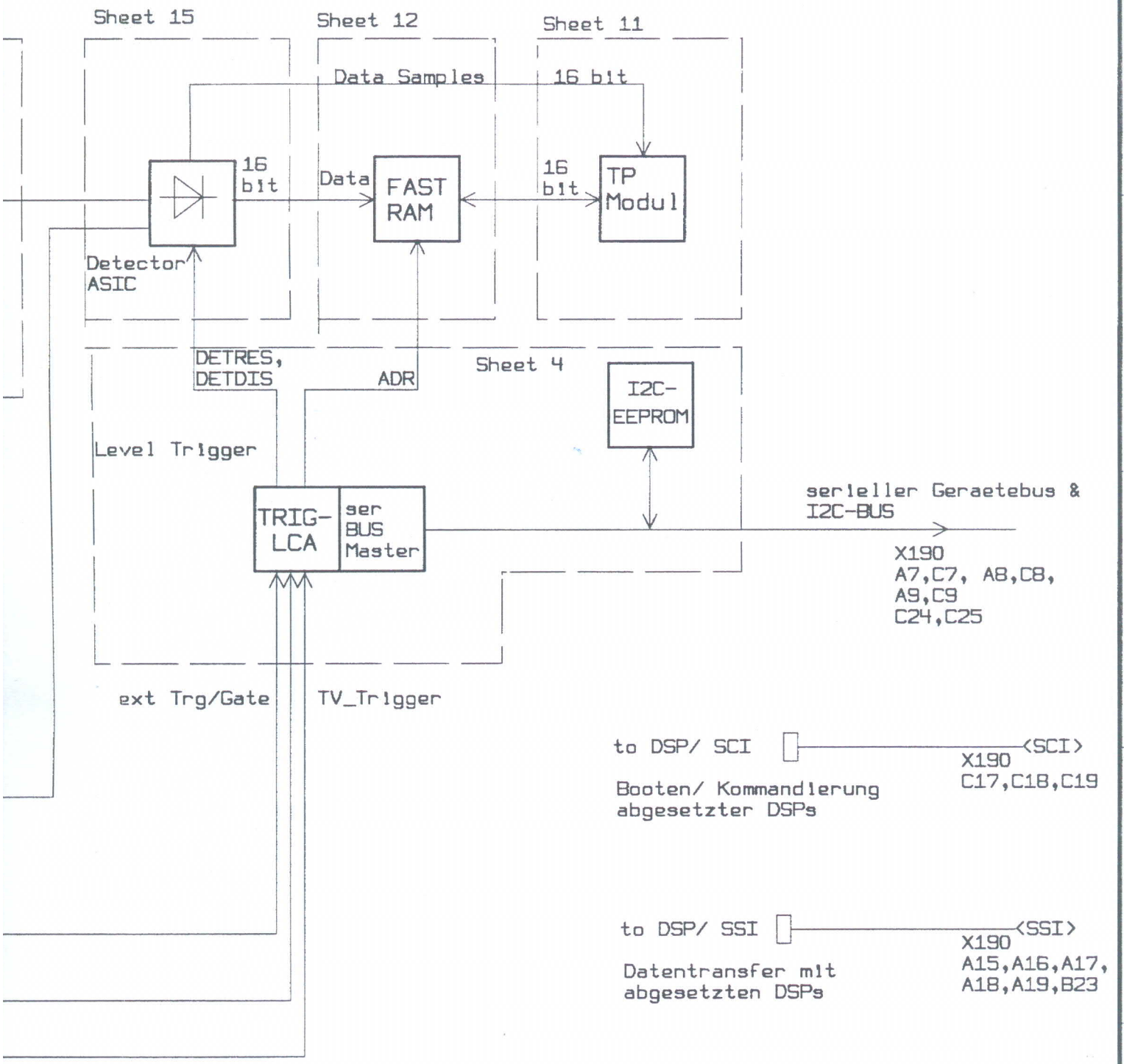

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BENENNUNG
DETECTOR_BOARD

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ROHDE&SCHWARZ

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BLATT-NR. 1
V. 2 BL.

ZU GERAET FSEA

REG.I.V. 1065.6000

ERSTE Z. 1065.6000

ROHDE&SCHWARZ

SERVICE DOCUMENTS
Digitales Motherboard

1065.6639.02

Contents

7 Testing the Module

7.1 Function Description

The digital motherboard provides slots for the modules Main CPU, Graphics, VGA, LAN as well as for an optional ISA plug-in card. The module accommodates the connectors for hard disk, drive, COM1/2 LPT, mouse, external montitor as well as for 1 IEC-bus interface and 1 bidirectional user port (2x8 bits). Besides, the control of the antenna coding socket, the front-panel keyboard and the front-panel LEDs as well as brightness control of the display are implemented on this module.
The digital motherboard can be subdivided into 5 functional blocks:

1) Modules and interfaces of the PC-compatible part
2) active I/O section:
   - 2 a) ISA interface of the active I/O section
   - 2 b) Front-panel control
   - 2 c) User port control
   - 2 d) IEC-bus interface

The active part of the module is exclusively controlled via I/O addresses of the Main CPU module.

The module occupies the following I/O addresses, interrupt lines and DMA channels:

Device	Addresses	IRQ	DMA	Write / read
IEC1	F020H - F027H	10;11	1	r/w
IEC-IRQ-logic reset	F030H - F031H	---	---	r/w
IEC-DMA-logic reset	F032H - F033H	---	---	r/w
DMA-TC-latch reset	F034H - F035H			r/w
PIO	F036H - F039H	---	---	r/w
Antenna coding socket (Probe Code)	F03AH - F03BH	19	---	w
LCD display latch	F03CH - F03DH	---	---	w
Front-panel LED latch	F03EH - F03FH	---	---	w
PERIF	F040H - F04FH	16;17	---	r/w
BG identification	F05EH - F05FH	---	---	r/w

7.1.1 Block Diagram

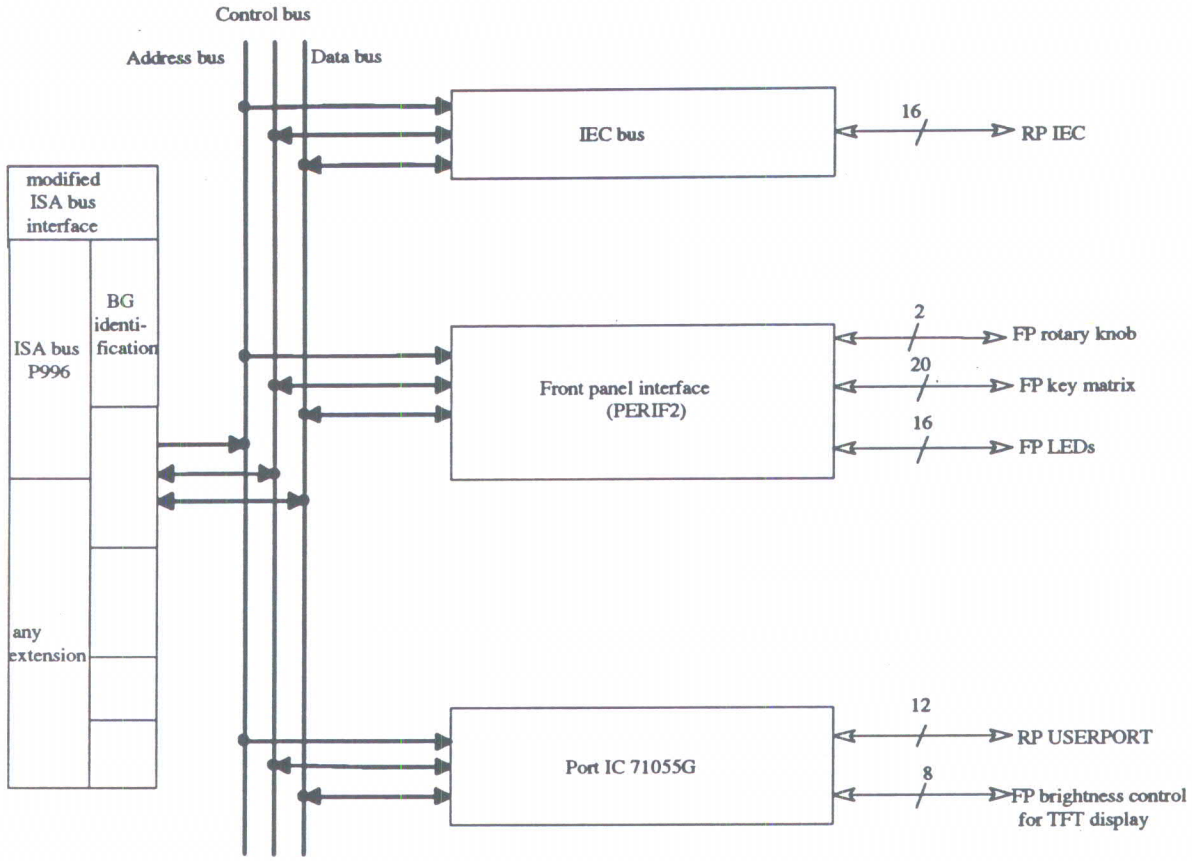

Fig. 1: Block diagram of the active part of the module

7.2 Measuring Instruments and Auxiliary Equipment

Item	Type of instrument	Specifications	Appropriate R&S device	Order no.	Use
1	Digital multimeter	0 to 20 V =	UDL35	1037.1807.02	- Measuring various levels - Checking passive connections

7.3 Troubleshooting

7.3.1 Error in the IEC-bus Interface

If the instrument can no longer be operated via the 24-pin IEC625 interface, check whether the fault lies in the hardware. To this end find out whether the cabling complies with the IEC625 standard - a maximum of 15 devices simultaneously connected to the bus, only one system controller, cable lengths accordingly.
The hardware can be regarded as functioning properly if, with the IEC-bus address set correctly (setting see section 2.4.6.2.1 FSE Operating Manual), the instrument responds to the **IDN?* command with the reply described in the Operating Manual in section 3.6.2 (Common Commands). If this is not the case and if the instrument works properly in manual mode, the fault lies in the Digital Motherboard. However, first check whether the plug-in cards in the ISA slots cause an address, interrupt or DMA conflict. The reserved ranges are described in section 7.1. The options VGA and LAN are factory-set to the appropriate configuration.
A fault in the Main CPU module also affects other instrument functions.
If a fault occurs with individual IEC-bus commands, this may be due to maloperation (not all commands are available for each instrument setup) or to other instrument errors. In these cases, it may be useful to evaluate the status registers of the interface (**ESR?* and **STB?*).

7.3.2 Fault in User Port

The User Port interface provides two bidirectional 8-bit ports that can be separately controlled. Direction and value (in the case of Output direction) can be set via normal instrument operation. Two main types of errors may occur at this interface:

- +5V voltage at pin 13 and 24 missing.
- one or both ports do not function properly or not at all.

The +5V voltage is generated on the Main CPU module. If it is missing, either this module is faulty or the connection on the motherboard is open. The output voltage can be measured at pin X301 A31.
Functioning of the user ports can be checked with the Input direction by connecting the individual line with instrument ground. **Open** pins must provide a "1", grounded pins a "0". It is **absolutely** necessary to select the Input as direction before. In the case of the Output direction, the "1" bits must feature a level of +5 V, the "0" bits 0 V.
If the instrument shows a fault at the user port only, replace the digital motherboard. In the case of additional errors at other digital interfaces, first make sure that the Main CPU module funtions properly before making a statement about the digital motherboard.
The user port can also be checked using the service routine *fse_io* . In the case of the user port, this functions as with the instrument software. Operation of the program is described in the Annex.

7.3.3 Error in the Front Panel Interface

Both the individual keys of the front panel and the rotary knob are controlled by a device on the digital motherboard. All LEDs except for the standby and trigger LED are likewise controlled by the digital motherboard.
For checking the front-panel keyboard and the LEDs, the test routine *fse_io* (see Annex) is used. When pressing a key in the *Keys* menu, its key code and labelling must be indicated. When rotating the rotary knob, the number of steps is indicated, the sign representing the direction of rotation. If no key code or no number of steps is indicated in this test, the signal path is open or there is a fault in the keyboard controller. In order to locate the fault, the row or column circuit corresponding to the key must be measured. The assignment of the keyboard matrix is to be obtained from the service manual of the front panel. When a key is pressed, the row circuit is connected with the respective column circuit. As the column signals from the keyboard controller are 0-V outputs in the idle state, it must be possible to measure this potential on the row signal upon a keystroke. If this is the case, the digital motherboard must be replaced. Row and column signals can be measured on the digital motherboard on connector X41.
The test routine *fse_io* also permits to switch on and off the LEDs except the trigger LED. If the LED is switched on, the corresponding signal must be applied to ground potential. The trigger LED can be

switched on via an AND operation both from the digital motherboard and from the detector. This is done either by the test routine or via ground potential applied to signal SWP_LED.

The assignment of the LED signals can be obtained from the following table:

Designation	Signal	Pin at X41
REMOTE	LED0	32
SRQ	LED1	33
HOLD	LED2	34
TRACE1	LED3	35
TRACE2	LED4	36
TRACE3	LED5	37
TRACE4	LED6	38
TRIGGER	LED7	39
SWT	LED8	40
VBW	LED9	41
RBW	LED10	42

7.3.4 Error in the Backlighting

The brightness of the backlighting is controlled by a register at address F03Ch. The value of this register can be measured using the signals LLUM4 to LLUM0 (connector X41). This value can be set in the *Backlight* menu of the test routine *fse_io*. If it does not comply with the signal states LLUM4 to LLUM0, there is a fault in the module. If the signal values are correct, but the brightness is not okay, the front panel must be checked.

7.3.5 Error in the Antenna Coding Socket (Probe Code)

The input signals of the antenna coding socket are read in by means of a parallel I/O device on the digital motherboard. The signals CODE7 to CODE0 are pulled to +5 V by pull-up resistors and must drop to 0 V at connector X41 in the case of ground connection at the front-panel socket. If this is the case and the decoding is not correctly identified, there is a fault in the digital motherboard.
The following table shows the assignment of the signals of the antenna coding socket at the front panel to the signals CODE7 to CODE0 on the digital motherboard.

Signal	Pin at Probe Code socket front panel
CODE0	M
CODE1	J
CODE2	H
CODE3	G
CODE4	F
CODE5	E
CODE6	D
CODE7	C

7.3.6 Fault in the PC Interfaces

If the PC-compatible interfaces COM1, COM2, LPT and the mouse do not function properly, refer to the Main CPU. The same is true if the hard disk and the disk drive do not work properly. The digital motherboard only procides a passive electrical connection for the interface between Main CPU and transputer graphics as well as between Main CPU and optional LAN or VGA card. Troubleshooting in these areas on the board itself is only possible by checking the connecting signals according to the signal assignment in section 7.5.

7.4 External Interfaces

OVERVIEW OF CONNECTORS

No.	Name	No.	Name
X35	VGABUS	X54	MONITOR
X38	HDBUS	X55	USER
X40	LCDBUS	X56	MOUSE
X41	FRONTP	X57	IEC1
X42	FDBUSv	X58	PSdigi
X43	FDBUSd	X59	Reset
X45	FAN2	X300	MPisa
X46	FAN1	X301	MPdata
X47	Sweep	X310	GRisa
X50	LPT	X311	GRLcd
X51	KEYBOARD	X330	Option
X52	COM1	X340	LAN
X53	COM2	X350	VGA

CONNECTOR X35 VGABUS for VGA↔GR (Pin 1 is at the right back)

Pin	Signal	Pin	Signal
1	NC	2	VGVSYNC9
3	GND_D	4	FPHDE9
5	NC	6	FPHDE
7	NC	8	FPVDCLK
9	NC	10	VGVSYNC
11	NC	12	VGHSYNC
13	GND_D	14	PNLOFF
15	GND_D	16	PD0
17	GND_D	18	PD1
19	GND_D	20	PD2
21	GND_D	22	PD3
23	GND_D	24	PD4
25	GND_D	26	PD5
27	GND_D	28	PD6
29	GND_D	30	PD7
31	GND_D	32	PD8
33	GND_D	34	PD9
35	GND_D	36	PD10
37	GND_D	38	PD11
39	GND_D	40	PD12
41	GND_D	42	PD13
43	NC	44	PD14
45	NC	46	PD15
47	NC	48	PD16
49	NC	50	PD17

CONNECTOR X38 HDBUS for HD (Pin 1 is at the right front)

Pin	Signal	Pin	Signal
1	RST-N	2	GND_D
3	HD7	4	HD8
5	HD6	6	HD9
7	HD5	8	HD10
9	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14

17	HD0	18	HD15
19	GND_D	20	NC
21	NC	22	GND_D
23	HIOW-N	24	GND_D
25	HIOR-N	26	GND_D
27	NC	28	IDEALE
29	NC	30	GND_D
31	INTRQ	32	IOCS16-N
33	HA1	34	PDIAG-N
35	HA0	36	HA2
37	HCS0-N	38	HCS1-N
39	DASP-N	40	GND_D
41	+5V_D	42	+5V_D
43	GND_D	44	NC

CONNECTOR X40 LCDBUS+TPLeft to analog motherboard (Pin 1 is at the left back)

Pin	Signal	Pin	Signal
1	SYSRESET	2	GND_D
3	LINK_F>G	4	LINK_G>F
5	GND_D	6	LINK_P>G
7	LINK_G>P	8	GND_D
9	LINK_P>A	10	LINK_A>P
11	GND_D	12	LINK_F>A
13	LINK_A>F	14	GND_D
15	ERROR1	16	+12V_Stby
17	LCDCLK	18	GND_D
19	LCDR0	20	LCDR1
21	LCDR2	22	GND_D
23	LCDG0	24	LCDG1
25	LCDG2	26	GND_D
27	LCDB0	28	LCDB1
29	LCDB2	30	GND_D
31	LCDHSYNC	32	GND_D
33	LCDVSYNC	34	GND_D
35	LCDENAB	36	ERROR2
37	ANALYSE	38	TRESET
39	VL5-P	40	VL12-P
41	PGOOD	42	+5V_D
43	+5V_D	44	+5V_D
45	+5V_D	46	+5V_D
47	+5V_D	48	+5V_D
49	+5V_D	50	+5V_D
51	+5V_D	52	SWEEP
53	ON	54	LCDHOS1
55	LCDHOS2	56	FANGND
57	FAN	58	SWP_LED
59	+28V_NS	60	NC
61	NC	62	NC
63	NC	64	NC

CONNECTOR X41 FRONTP for FP-Hardkeys (Pin 1 front left)

Pin	Signal	Pin	Signal
1	GND_D	2	+5V_D
3	RMKDIR	4	RMKPULS
5	ROW0	6	ROW1
7	ROW2	8	ROW3
9	ROW4	10	ROW5
11	ROW6	12	ROW7
13	COL0	14	COL1
15	COL2	16	COL3
17	COL4	18	COL5
19	COL6	20	COL7
21	COL8	22	COL9
23	COL10	24	COL11
25	ON	26	+12V_Stby
27	LLUM0	28	LLUM1
29	LLUM2	30	LLUM3

31	LLUM4	32	LED0
33	LED1	34	LED2
35	LED3	36	LED4
37	LED5	38	LED6
39	LED7	40	LED8
41	LED9	42	LED10
43	LED11	44	LED12
45	LED13	46	LED14
47	LED15	48	GND_D
49	CODE0	50	CODE1
51	CODE2	52	CODE3
53	CODE4	54	CODE5
55	CODE6	56	CODE7
57	+5V_D	58	SPOUT
59	+12V_D	60	+12V_D
61	+12V_D	62	+12V_D
63	GND_D	64	GND_D

CONNECTOR X42 FDBUS voltage supply for FD (Pin 1 at the back)

Pin	Signal
1	+5V
2	GND_D
3	GND_D
4	NC

CONNECTOR X43 FDBUS data for FD (Pin 1 front left)

Pin	Signal	Pin	Signal
1	NC	2	HDIN
3	NC	4	NC
5	NC	6	NC
7	GND_D	8	INDEX
9	GND_D	10	MOTORON0
11	GND_D	12	DRIVESEL0
13	GND_D	14	DRIVESEL1
15	GND_D	16	MOTORON1
17	GND_D	18	DIRECTIONSEL
19	GND_D	20	STEPFD
21	GND_D	22	WRITEDATA
23	GND_D	24	WRITEGATE
25	GND_D	26	TRACK00
27	GND_D	28	WRITEPROTECT
29	GND_D	30	READDATA
31	GND_D	32	SIDEONESEL
33	GND_D	34	DISKCHANGE

CONNECTOR X45 FAN2 (Pin 1 is at the left)

Pin	Signal
1	FAN
2	FANGND

CONNECTOR X46 FAN1 (Pin 1 is at the left)

Pin	Signal
1	FAN
2	FANGND

CONNECTOR X47 Sweep (Pin 1 is at the left)

Pin	Signal
1	FAN
2	FANGND
3	+28V_NS
4	NC

CONNECTOR X50 LPT (Pin 1 front right)

Pin	Signal	Pin	Signal
1	STROBE-N		
2	D0	14	AUTOFE-N
3	D1	15	ERROR-N
4	D2	16	LPTINIT-N
5	D3	17	SLCTIN-N
6	D4	18	GND_D
7	D5	19	GND_D
8	D6	20	GND_D
9	D7	21	GND_D
10	ACK-N	23	GND_D
11	BUSY	24	GND_D
12	PE	25	GND_D
13	SLCT		

CONNECTOR X51 KEYBOARD (Pin 1 front left)

Pin	Signal	Pin	Signal
1	KBDCLK	4	KBDVD5
2	KBDDATA	5	KBDINH
3	KBDGND		

CONNECTOR X52 COM1 (Pin 1 front left)

Pin	Signal	Pin	Signal
1	DCD1	2	RXD1
3	TXD1	4	DTR1
5	GND_D	6	DSR1
7	RTS1	8	CTS1
9	RI1		

CONNECTOR X53 COM2 (Pin 1 front left)

Pin	Signal	Pin	Signal
1	DCD2	2	RXD2
3	TXD2	4	DTR2
5	GND_D	6	DSR2
7	RTS2	8	CTS2
9	RI2		

CONNECTOR X54 MONITOR (Pin 1 front right)

Pin	Signal	Pin	Signal
1	MONR	2	MONG
3	MONB	4	NC
5	GND_D	6	GNDMON
7	GNDMON	8	GNDMON
9	NC	10	GND_D
11	NC	12	NC
13	MONHSYNC	14	MONVSYNC
15	NC	16	NC

CONNECTOR X55 USER (Pin 1 front right)

Pin	Signal	Pin	Signal
1	USRPA0	14	USRPC0
2	USRPA1	15	USRPC1
3	USRPA2	16	USRPC2
4	USRPA3	17	USRPC3
5	USRPA4	18	USRPC4
6	USRPA5	19	USRPC5
7	USRPA6	20	USRPC6
8	USRPA7	21	USRPC7
9	GND_D	22	NC
10	GND_D	23	NC
11	GND_D	24	SPVD5
12	GND_D	25	NC
13	SPVD5		

CONNECTOR X56 MOUSE (Pin 1 back right)

Pin	Signal	Pin	Signal
1	MOUSECLK	4	MOUSEVD5
2	MOUSEGND	5	NC
3	MOUSEDATA	6	NC

CONNECTOR X57 IEC1 (Pin 1 front right)

Pin	Signal	Pin	Signal
1	IEC1D1	13	IEC1D5
2	IEC1D2	14	IEC1D6
3	IEC1D3	15	IEC1D7
4	IEC1D4	16	IEC1D8
5	IEC1EOI	17	IEC1REN
6	IEC1DAV	18	GND_D
7	IEC1NRFD	19	GND_D
8	IEC1NDAC	20	GND_D
9	IEC1IFC	21	GND_D
10	IEC1SRQ	22	GND_D
11	IEC1ATN	23	GND_D
12	GND_D	24	GND_D

CONNECTOR X58 digital supply voltages from PS (Pin1 front right)

Pin	Signal	Pin	Signal	Pin	Signal
1	+5V_D	4	GND_D	7	GND_D
2	+5V_D	5	+12V_Stby	8	GND_D
3	+5V_D	6	+12V_D	9	GND_D

CONNECTOR X59 RESET (Pin 1 left)

Pin	Signal	Pin	Signal
1	RESET-N	2	GND_D

CONNECTOR X300 for MP (MPisa) (Pin A1 back left)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A 1	GND_D	B 1	IOR-N	C 1	GND_D	D 1	GND_D
A 2	+5V_D	B 2	IOW-N	C 2	+5V_D	D 2	GND_D
A 3	NC	B 3	MEMR-N	C 3	VD12-N	D 3	GND_D
A 4	BALE	B 4	MEMW-N	C 4	SBHE-N	D 4	NC (res. IRQ20)
A 5	SA0	B 5	NC(res. LACHn)	C 5	SA1	D 5	+5V_D
A 6	SA2	B 6	GND_D	C 6	SA3	D 6	+5V_D
A 7	SA4	B 7	SA5	C 7	SA6	D 7	+5V_D
A 8	SA7	B 8	SA8	C 8	SA9	D 8	NC (res. IRQ21)
A 9	SA10	B 9	SA11	C 9	SA12	D 9	NC (res. IRQ22)
A 10	SA13	B 10	SA14	C 10	SA15	D 10	NC (res. IRQ23)
A 11	SA16	B 11	LA17	C 11	LA18	D 11	SA17
A 12	LA19	B 12	LA20	C 12	LA21	D 12	SA18
A 13	LA22	B 13	LA23	C 13	IRQ3	D 13	SA19
A 14	IRQ4	B 14	IRQ5	C 14	IRQ6	D 14	SMEMR-N
A 15	IRQ7	B 15	IRQ9	C 15	IRQ10	D 15	SMEMW-N
A 16	IRQ11	B 16	IRQ12	C 16	IRQ14	D 16	LA24
A 17	IRQ15	B 17	IOCHCHK-N	C 17	DRQ0	D 17	LA25
A 18	DRQ1	B 18	DRQ2	C 18	DRQ3	D 18	LA26
A 19	DRQ5	B 19	DRQ6	C 19	DRQ7	D 19	IRQ16
A 20	DACK0-N	B 20	GND_D	C 20	DACK1-N	D 20	IRQ17
A 21	DACK2-N	B 21	DACK3-N	C 21	DACK5-N	D 21	IRQ18
A 22	DACK6-N	B 22	DACK7-N	C 22	TC	D 22	IRQ19
A 23	SD0	B 23	SD1	C 23	SD2	D 23	LA31
A 24	SD3	B 24	+5V_D	C 24	SD4	D 24	OSC
A 25	SD5	B 25	SD6	C 25	SD7	D 25	
A 26	SD8	B 26	SD9	C 26	SD10	D 26	+5V_D
A 27	SD11	B 27	SD12	C 27	SD13	D 27	+5V_D
A 28	SD14	B 28	SD15	C 28	IOCHRDY	D 28	+5V_D
A 29	AEN	B 29	MEMCS16-N	C 29	IOCS16-N	D 29	

A 30	RESETDRV	B 30	ENDXFR-N	C 30	MASTER-N	D 30	GND_D
A 31	+5V_D	B 31	REFRESH-N	C 31	+5V_D	D 31	GND_D
A 32	GND_D	B 32	SYSCLK	C 32	GND_D	D 32	GND_D

CONNECTOR X301 for MP (MPdata) (Pin A1 back left)

Pin	Signal	Pin	Signal	Pin	Signal
A 1	HDIN	B 1	STROBE-N	C 1	DCD1
A 2	INDEX	B 2	D0	C 2	RXD1
A 3	MOTORON0	B 3	D1	C 3	TXD1
A 4	DRIVESEL0	B 4	D2	C 4	DTR1
A 5	DRIVESEL1	B 5	D3	C 5	DSR1
A 6	MOTORON1	B 6	D4	C 6	RTS1
A 7	DIRECTIONSEL	B 7	D5	C 7	CTS1
A 8	STEPFD	B 8	D6	C 8	RI1
A 9	WRITEDATA	B 9	D7	C 9	DCD2
A 10	WRITEGATE	B 10	ACK-N	C 10	RXD2
A 11	TRACK00	B 11	BUSY	C 11	TXD2
A 12	WRITEPROTECT	B 12	PE	C 12	DTR2
A 13	READDATA	B 13	SLCT	C 13	DSR2
A 14	SIDEONESEL	B 14	AUTOFE-N	C 14	RTS2
A 15	DISKCHANGE	B 15	ERROR-N	C 15	CTS2
A 16	LPTINIT-N	B 16	SLCTIN-N	C 16	RI2
A 17		B 17	DASP-N	C 17	GND_D
A 18		B 18	HCS0-N	C 18	HCS1-N
A 19	RESET-N	B 19	HA0	C 19	HA2
A 20	SYSRESET	B 20	HA1	C 20	PDIAG-N
A 21	MOUSECLK	B 21	INTRQ	C 21	IOCS16-N
A 22	KBDCLK	B 22	HIOR-N	C 22	GND_D
A 23	KBDDATA	B 23	HIOW-N	C 23	IDEALE
A 24	KBDGND	B 24	HD0	C 24	HD15
A 25	KBDVD5	B 25	HD1	C 25	HD14
A 26	KBDINH	B 26	HD2	C 26	HD13
A 27	MOUSEDATA	B 27	HD3	C 27	HD12
A 28	MOUSEGND	B 28	HD4	C 28	HD11
A 29	MOUSEVD5	B 29	HD5	C 29	HD10
A 30	SPOUT	B 30	HD6	C 30	HD9
A 31	SPVD5	B 31	HD7	C 31	HD8
A 32	NC	B 32	RST-N	C 32	GND_D

CONNECTOR X310 for GR (GRisa) (Pin A1 front left)

Pin	Signal	Pin	Signal	Pin	Signal
A 1	GND_D	B 1	IOR-N	C 1	GND_D
A 2	+5V_D	B 2	IOW-N	C 2	+5V_D
A 3	+12V_D	B 3	MEMR-N	C 3	-12V_D
A 4	BALE	B 4	MEMW-N	C 4	SBHE-N
A 5	SA0	B 5	NC	C 5	SA1
A 6	SA2	B 6	GND_D	C 6	SA3
A 7	SA4	B 7	SA5	C 7	SA6
A 8	SA7	B 8	SA8	C 8	SA9
A 9	SA10	B 9	SA11	C 9	SA12
A 10	SA13	B 10	SA14	C 10	SA15
A 11	SA16	B 11	LA17	C 11	LA18
A 12	LA19	B 12	LA20	C 12	LA21
A 13	LA22	B 13	LA23	C 13	IRQ3
A 14	IRQ4	B 14	IRQ5	C 14	IRQ6
A 15	IRQ7	B 15	IRQ9	C 15	IRQ10
A 16	IRQ11	B 16	IRQ12	C 16	IRQ14
A 17	IRQ15	B 17	IOCHCHK-N	C 17	DRQ0
A 18	DRQ1	B 18	DRQ2	C 18	DRQ3
A 19	DRQ5	B 19	DRQ6	C 19	DRQ7
A 20	DACK0-N	B 20	GND_D	C 20	DACK1-N
A 21	DACK2-N	B 21	DACK3-N	C 21	DACK5-N
A 22	DACK6-N	B 22	DACK7-N	C 22	TC
A 23	SD0	B 23	SD1	C 23	SD2
A 24	SD3	B 24	+5V_D	C 24	SD4
A 25	SD5	B 25	SD6	C 25	SD7
A 26	SD8	B 26	SD9	C 26	SD10

A 27	SD11	B 27	SD12	C 27	SD13
A 28	SD14	B 28	SD15	C 28	IOCHRDY
A 29	AEN	B 29	MEMCS16-N	C 29	IOCS16-N
A 30	RESETDRV	B 30	ENDXFR-N	C 30	MASTER-N
A 31	+5V_D	B 31	REFRESH-N	C 31	+5V_D
A 32	GND_D	B 32	SYSCLK	C 32	GND_D

CONNECTOR X311 for GR (GRLcd) (Pin A1front left)

Pin	Signal	Pin	Signal	Pin	Signal
A 1	VL5-P	B 1	VL12-P	C 1	
A 2		B 2		C 2	
A 3	DISPLAYON	B 3		C 3	8514ON
A 4	OPLNKO1	B 4		C 4	OPLNKO2
A 5	OPLNKI1	B 5		C 5	OPLNKI2
A 6	GND_D	B 6	GND_D	C 6	GND_D
A 7	PD9	B 7	PD10	C 7	PD11
A 8	PD12	B 8	PD13	C 8	PD14
A 9	PD15	B 9	PD16	C 9	PD17
A 10	VGHSYNC	B 10		C 10	VGVSYNC
A 11	PD0	B 11	PD1	C 11	PD2
A 12	PD3	B 12	PD4	C 12	PD5
A 13	PD6	B 13	PD7	C 13	PD8
A 14	FPVDCLK	B 14		C 14	FPHDE
A 15	MONHSYNC	B 15	PNLOFF	C 15	MONVSYNC
A 16	MONR	B 16	MONG	C 16	MONB
A 17	GNDMON	B 17	GNDMON	C 17	GNDMON
A 18	GND_D	B 18	GND_D	C 18	GND_D
A 19	LINK_F>G	B 19	LINK_P>G	C 19	ANALYSE
A 20	LINK_G>F	B 20	LINK_G>P	C 20	ERROR1
A 21	LINK_F>A	B 21	LINK_P>A	C 21	ERROR2
A 22	LINK_A>F	B 22	LINK_A>P	C 22	TRESET
A 23	GND_D	B 23	GND_D	C 23	GND_D
A 24	LCDCLK	B 24		C 24	
A 25	LCDR0	B 25	LCDR1	C 25	LCDR2
A 26	NC	B 26	NC	C 26	NC
A 27	LCDG0	B 27	LCDG1	C 27	LCDG2
A 28	NC	B 28	NC	C 28	NC
A 29	LCDB0	B 29	LCDB1	C 29	LCDB2
A 30	NC	B 30	NC	C 30	NC
A 31	LCDHSYNC	B 31	LCDVSYNC	C 31	LCDENAB
A 32	GND_D	B 32	GND_D	C 32	GND_D

CONNECTOR X330, X340, X350 for Option, LAN and VGA (Pin A1 front left)

Pin	Signal	Pin	Signal
A 1	IOCHCHK-N	B 1	GND_D
A 2	SD7	B 2	RESETDRV
A 3	SD6	B 3	+5V_D
A 4	SD5	B 4	IRQ9
A 5	SD4	B 5	NC
A 6	SD3	B 6	DRQ2
A 7	SD2	B 7	-12V_D
A 8	SD1	B 8	ENDXFR-N
A 9	SD0	B 9	+12V_D
A 10	IOCHRDY	B 10	GND_D
A 11	AEN	B 11	SMEMW-N
A 12	SA19	B 12	SMEMR-N
A 13	SA18	B 13	IOW-N
A 14	SA17	B 14	IOR-N
A 15	SA16	B 15	DACK3-N
A 16	SA15	B 16	DRQ3
A 17	SA14	B 17	DACK1-N
A 18	SA13	B 18	DRQ1
A 19	SA12	B 19	REFRESH-N
A 20	SA11	B 20	SYSCLK
A 21	SA10	B 21	IRQ7

A 22	SA9	B 22	IRQ6
A 23	SA8	B 23	IRQ5
A 24	SA7	B 24	IRQ4
A 25	SA6	B 25	IRQ3
A 26	SA5	B 26	DACK2
A 27	SA4	B 27	TC
A 28	SA3	B 28	BALE
A 29	SA2	B 29	+5V_D
A 30	SA1	B 30	OSC
A 31	SA0	B 31	GND_D

C 1	SBHE-N	D 1	MEMCS16-N
C 2	LA23	D 2	IOCS16-N
C 3	LA22	D 3	IRQ10
C 4	LA21	D 4	IRQ11
C 5	LA20	D 5	IRQ12
C 6	LA19	D 6	IRQ15
C 7	LA18	D 7	IRQ14
C 8	LA17	D 8	DACK0-N
C 9	MEMR-N	D 9	DRQ0
C 10	MEMW-N	D 10	DACK5-N
C 11	SD8	D 11	DRQ5
C 12	SD9	D 12	DACK6-N
C 13	SD10	D 13	DRQ6
C 14	SD11	D 14	DACK7-N
C 15	SD12	D 15	DRQ7
C 16	SD13	D 16	+5V_D
C 17	SD14	D 17	MASTER-N
C 18	SD15	D 18	GND_D

7.5 Annex

Service routine fse_io.exe

The routine is to be found on the service disk and is started after the instrument has booted from this disk.

Caution: The test routine must not be started with the instrument software running !

After the program has been started, the main menu with the individual test groups appears (front panel, LEDs, User Port). Input of the respective digit allows to change to the desired menu. The ESC key permits to enter the main menu from the submenus. The ESC key terminates the program in the main menu. Besides, it can also be aborted at any time by pressing CONTROL-C.

Front-panel menu:
On pressing of a key or rotation of the rotary knob, the value of the interrupt register in the keyboard controller is displayed in the field *Interrupt*.
The designation of the key is indicated in the field *Key*, the key code in the field *Code* (according to the table in the service manual of the front panel). In the case of a fault, the message *column error* or *row error* is displayed.
In the field *Rollkey*, the number and direction of the steps are indicated after turning the rotary knob.

LEDs menu:
By entering the digit for the desired LED, its status can be switched over. At the beginning, all LEDs except the trigger LED are switched off. The trigger LED can only be checked if the line SWP_LED (connector X40) is applied to ground potential.

Backlight menu:
By entering a number between 0 and 31, the brightness of the backlighting can be set. 0 corresponds to the OFF state and 31 corresponds to maximum brightness. When the program is started, the brightness is set to maximum in order to ensure reliable ignition of the tubes.

User Port menu:
As with the instrument function, this menu permits to write or read user port values. In addition, the status of the signal lines is polled and indicated at the antenna coding socket when reading.
The user port values are entered in hexadecimal format.

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SERVICE DOCUMENTS
Frontpanel

1065.6251.02

Contents

7 Testing the Module

7.1 Function Description

The front panel consists of:

- Membrane keyboard with LEDs,
- Standby switch,
- Liquid crystal display with DC/AC converter,
- Display module,
- Female connector PROBE / CODE.

The display module comprises the rotary knob and the brightness control for the LCD backlighting. In addition, it constitutes the connection from the membrane keyboard (including LEDs) and the female connector PROBE / CODE to the digital motherboard.

7.2 Measuring Instruments and Auxiliary Equipment

Item	Type of Instrument	Specifications	Appropriate R&S device	Order no.	Use
1	Digital voltmeter	0 to 20 V =	UDL35	1037.1807.02	- Testing the backlighting

7.3 Troubleshooting

7.3.1 Problems with the Keyboard or the Rotary Knob

If individual or all keys do not work or if the rotary knob does not respond, the test routine described in the chapter about the digital motherboard should be used for troubleshooting. To allow for fault location, the section "Interfaces" includes a table containing the assignment of the keyboard connectors.

7.3.2 Problems with the Standby Pushbutton

The Standby pushbutton generates the Power ON signal which is directly applied to the power supply. With the pushbutton depressed (switch position ON), this signal must be applied to ground potential. With the switch set to STANDBY, the signal is not connected and is pulled to high by a pull-up resistor in the power supply. The Power ON signal is to be found on connector X1 at pin 25.
The standby pushbutton is designed as switch and controls both the Power ON signal and the LEDs STANDBY and ON via a bias resistor each.

7.3.3 Problems with Backlighting

If the backlighting remains dark, if it is unevenly bright or flickers, either the backlighting itself or the backlighting control may be faulty. If the backlighting consists of two tubes and if the fault only occurs in one of them, this tube is most likely to be faulty. If, however, both tunbes do not work or if there is only one tube, the DC/AC converter should be checked next.
The converter is either part of the backlighting or accommodated in an extra housing between display module and display. The converter uses a DC voltage at the input to generate an AC voltage for control of the tubes. This AC voltage features a frequency of approx. 30 kHz and ranges between 1000 V before ignition and about 300 V to 500 V during operation of the tubes. It does not make sense to check the output voltage of the converter for troubleshooting. However, the DC voltage at the converter input should be checked. This DC voltage is generated from the digital 12-V supply voltage. The converter input voltage can be set in the range from 7.7 V to 12 V via a D/A converter with a following series transistor as control element. This is done using the signals LLUM0 to LLUM4 generated on the digital motherboard and to be found on connector X1 at pin 27 to 31.

LLUM0	LLUM1	LLUM2	LLUM3	LLUM4	Input voltage of converter
L	L	x	x	x	0 V
L	H	L	L	L	7.7 V
L	H	H	L	L	8.4 V
H	L	L	L	L	9.2 V
H	L	H	L	L	9.9 V
H	H	L	L	L	10.7 V
H	H	H	L	L	11.4 V
H	H	H	H	H	12 V

The voltage should be measured once with connected converter and once in parallel to an equivalent resistance (approx. 20 ohms). The voltage can be adjusted using adjusting control R5.
The brightness can be controlled via the instrument software. After switching on the instrument, the backlighting is always set to full brightness first, because this is necessary to ensure reliable ignition of the tubes.

7.3.4 Problems with the PROBE / CODE Connector

The input signals of the PROBE / CODE connector are filtered on the display module and then taken to the digital motherboard. The two supply voltages +10 V and -10 V are derived from the analog motherboard. If the electrical connection via the display module is okay, the troubleshooting procedure is to be continued on the digital or analog motherboard.

7.4 External Interfaces

Key	ROW	X5.Pin	COL	X5.Pin	Code
SYSTEM-PRESET	5	6	8	17	58H
SYSTEM-CAL	4	5	8	17	48H
SYSTEM-DISPLAY	6	7	8	17	68H
SYSTEM-INFO	4	5	9	18	49H
CONFIGURATION-MODE	5	6	9	18	59H
CONFIGURATION-SETUP	6	7	9	18	69H
HARDCOPY-SETTINGS	4	5	10	19	4AH
HARDCOPY-START	5	6	10	19	5AH
STATUS-LOCAL	6	7	10	19	6AH
USER	0	1	0	9	00H
SOFTKEY 1	0	1	1	10	01H
SOFTKEY 2	0	1	2	11	02H
SOFTKEY 3	0	1	3	12	03H
SOFTKEY 4	0	1	4	13	04H
SOFTKEY 5	0	1	5	14	05H
SOFTKEY 6	0	1	6	15	06H
SOFTKEY 7	0	1	7	16	07H
SOFTKEY 8	0	1	8	17	08H
SOFTKEY 9	0	1	9	18	09H
SOFTKEY 10	0	1	10	19	0AH
FREQUENCY-CENTER	1	2	0	9	10H
FREQUENCY-START	1	2	1	10	11H
MARKER-NORMAL	1	2	3	12	13H
MARKER-DELTA	1	2	4	13	14H
TRACE-1	1	2	5	14	15H
TRACE-3	1	2	6	15	16H
MENU-UP	2	3	9	18	29H

MENU-LEFT	1	2	10	19	1AH
FREQUENCY-SPAN	2	3	0	9	20H
FREQUENCY-STOP	2	3	1	10	21H
MARKER-SEARCH	2	3	3	12	23H
MARKER-MKR→	2	3	4	13	24H
TRACE-2	2	3	5	14	25H
TRACE-4	2	3	6	15	26H
MENU-RIGHT	2	3	10	19	2AH
LEVEL-REF	7	8	0	9	70H
LEVEL-RANGE	7	8	1	10	71H
LINES-D LINES	7	8	3	12	73H
LINES-LIMITS	7	8	4	13	74H
SWEEP-TRIGGER	7	8	5	14	75H
SWEEP-SWEEP	7	8	6	15	76H
SWEEP-COUPLING	7	8	10	19	7AH
DATA INPUT-7	6	7	0	9	60H
DATA INPUT-4	6	7	1	10	61H
DATA INPUT-1	6	7	2	11	62H
DATA INPUT-0	6	7	3	12	63H
DATA INPUT-CLR	5	6	4	13	54H
DATA VARIATION-HOLD	6	7	5	14	65H
DATA INPUT-8	5	6	0	9	50H
DATA INPUT-5	5	6	1	10	51H
DATA INPUT-2	5	6	2	11	52H
DATA INPUT-'.'	5	6	3	12	53H
DATA VARIATION-STEP	5	6	5	14	55H
DATA INPUT-9	4	5	0	9	40H
DATA INPUT-6	4	5	1	10	41H
DATA INPUT-3	4	5	2	11	42H
DATA INPUT-'-'	4	5	3	12	43H

DATA INPUT-BACK	4	5	4	13	44H
DATA VARIATION-UP	3	4	5	14	35H
DATA VARIATION-LEFT	4	5	5	14	45H
DATA VARIATION-DOWN	4	5	6	15	46H
DATA INPUT-GHz	3	4	0	9	30H
DATA INPUT-MHz	3	4	1	10	31H
DATA INPUT-kHz	3	4	2	11	32H
DATA INPUT-Hz	3	4	3	12	33H
DATA INPUT-Exp	3	4	4	13	34H
DATA VARIATION-RIGHT	3	4	6	15	36H
MEMORY-CONFIG	3	4	7	16	37H
MEMORY-SAVE	3	4	8	17	38H
MEMORY-RECALL	3	4	9	18	39H
MEMORY-INPUT	3	4	10	19	3AH

Configuration of keyboard matrix and assignment of connector X5 on the display module

X6.Pin:	3	4	5	6	11	12	13
Cathode of LED	ON	STANDBY	REMOTE	SRQ	HOLD	TRACE 1	TRACE 2

X6.Pin:	14	15	17	18	19	20
Cathode of LED	TRACE 3	TRACE 4	TRIGGER	SWT	VBW	RBW

The terminals of the LEDs are to be found on connector X6. The anode of the ON-LED is applied to pin 2, all other LEDs are commonly applied to pin 1.

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Service documents

POWER SUPPLY

1043.9941.02

Contents

7 Testing the Module

7.1 Function Description of the Module

7.1.1 Function inside the Instrument

Main functions:

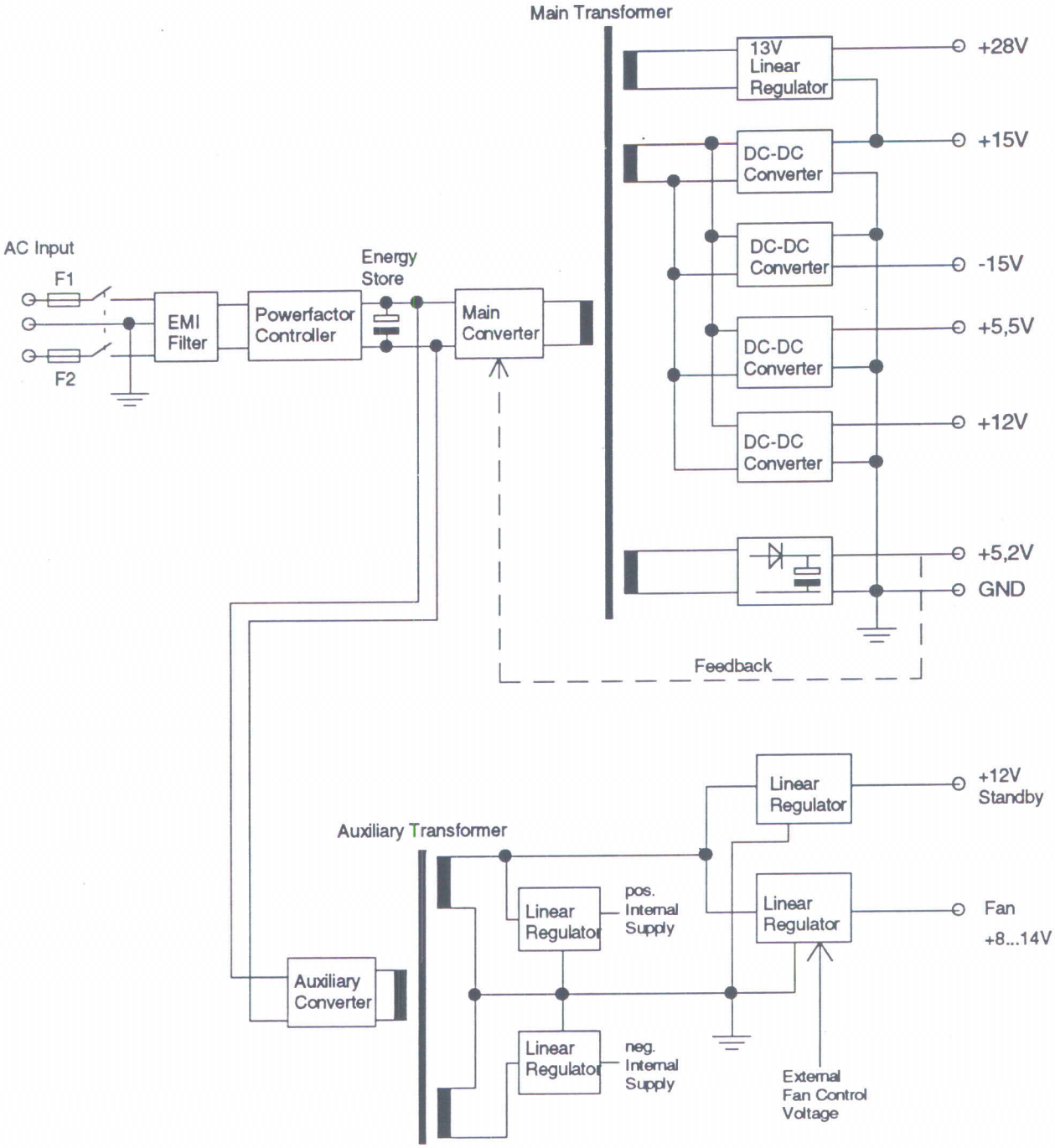
- Current supply of all modules.
- Temperature-controlled supply of the fans.
- Generation of the switch-on reset for the connected hardware.
- Generation of a line-synchronous trigger signal.

7.1.2 Description of the Block Diagram

The module involved is a primarily clocked switching power supply. The AC voltage is first rectified and up-converted to a voltage of 390 V via the power factor controller (PFC). The PFC generates a sine-shaped current at the input.
The DC voltage is applied to a converter, which generates three secondary voltages via the main transformer. The converter is used to adjust the 5.2-V output. The two remaining transformer windings provide an intermediate voltage of 42 V and the voltage for the 13-V linear regulator.
The intermediate voltage supplies several DC-DC converters, which serve to stabilize the desired output voltages.
To obtain the 28-V output voltage, the voltage of the 13-V linear regulator is added to the +15-V output voltage.

The auxiliary converter generates the supply voltages for the regulators and the monitoring circuits as well as the standby and the fan voltage.

Block diagram



7.1.3 Important Characteristics and Data

AC supply input

Voltage range: 90 VAC to 264 VAC continuous without switchover
Frequency: 47 to 440 Hz up to 32 V
47 to 66 Hz above 132 V

Undervoltage shutdown: the power supply switches off at <90 VAC (typ. 85 VAC).

States of operation

Off = Power switch off (disconnection from the AC supply)

Standby = AC supply voltage applied, power switch on, standby switch off

On = AC supply voltage applied, power switch on, standby switch on

Output voltages

No.	Connector	Vo V(DC)	stat. control Δ V(DC)	Current limiting A(DC)
1	X21.10	+28	+27to29	0.4 to 0.6 up to 15V 0.4 to 9.1 up to 0V
2	X21.5/6	+15	14.9 to 15.1	7.2 to 9.1
3	X23.5	+12 Standby	11.7 to 12.3	0.3 to 0.42
4	X23.6	+12	11.7 to 12.3	3.8 to 4.8
5	X21.1/2	+5.5	5.45 to 5.55	4.1 to 5.2 *)
6	X23.1-3	+5.2	5.15 to 5.25	18 to 22.9
7	X21.8	-15	-14.9 to -15.1	2.5 to 3.3
8	X20.10	+8 to 14.5 FAN	at 30°: 7.5 to 8.5 at 76°: 14 to 15	1.0 to 1.2

*) 3,1...3,8 until serial No. xxxxxx.xxx

Tab. 7.1.3_1

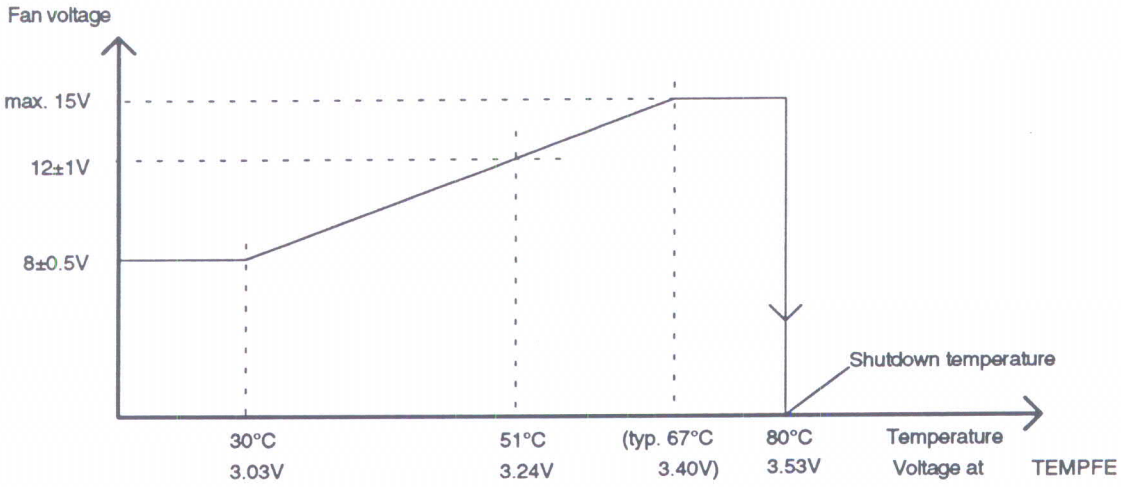
Minimum load

The power supply requires the following minimum load for proper functioning:
2 A for output +5.2 V
0.1 A for output +15 V

Fan control

The internal fans of the power supply are adjusted according to the internal temperature of the power supply.

The fan voltage FAN for the external fans is adjusted independently according to an external control voltage (by a temperature sensor in the FSE)



Temperature monitoring

The power supply is switched off in the case of overtemperature.
It is switched off:
a) in the case of overtemperature inside the power supply (100°C at heat sink of PFC)
b) in the case of overtemperature inside the instrument
The temperature inside the instrument is monitored by the temperature sensor to be connected to TEMPFE and TEMPFEGND. The power supply is switched off at 80°C (3.53 V). It can be switched on again when the temperature has cooled down to 75°C (3.48 V).

Shutdown as a result of the temperature voltage at TEMPFE does not take place if X20.12 is applied to ground.

Output voltage monitoring / overvoltage protection

If (1.15 to 1.25) x nominal voltage of an output is exceeded, the power supply immediately switches off all outputs. Switching on again is only possible after actuation of the power switch.
The outputs 12V Standby and fan voltage (FAN) are not equipped with an overvoltage protection.

When the voltage falls below (0.89 to 0.95) x nominal voltage of an output, the power supply switches off all outputs after approx. 5 s.
If X20.12 is applied to ground, there is no shutdown in the case of undervoltage.

Current limiting

When the outputs are overloaded, current limiting becomes effective, preventing the current from rising further. The values can be obtained from the table 7.1.3_1.

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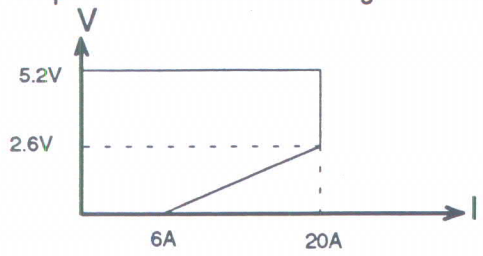
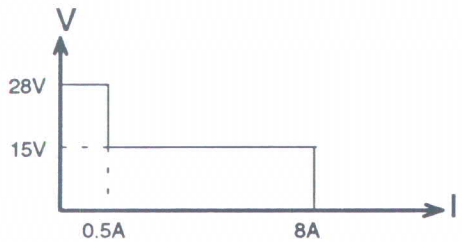
Particular features:
Output 6 features the following current-limiting characteristic.



Output 1 features the following current-limiting characteristic.



Shutdown in the case of an error

If an output is overloaded or short-circuited or can no longer be used due to a fault in the power supply and if this status continues for more than 5 to 15 s, all outputs are switched off.
This shutdown does not take place if the control input X20.12 is connected to GND.

Operating status signals

PGOOD

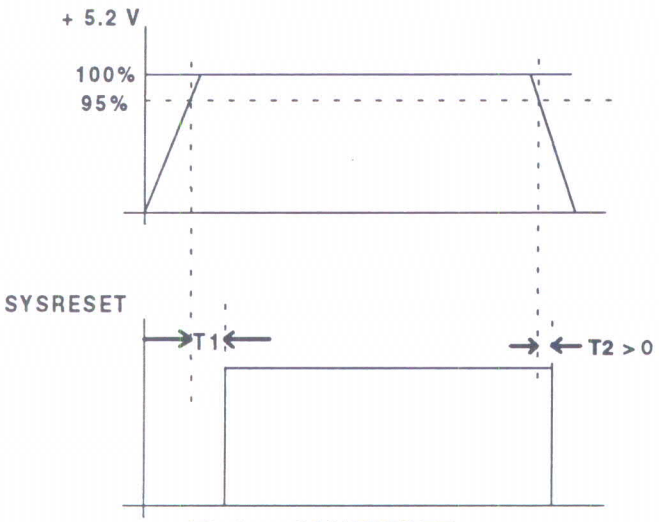
On switching on, the PGOOD signal switches from High to Low (HCT logic level) after all output voltages have reached 90% of their nominal value.
The PGOOD signal switches from Low to High as soon as an output voltage drops below 90% of its nominal value.
The fan voltage No. 8 is not monitored.

LED display
The LED in the rear panel of the power supply is illuminated simultaneously with the Low status of the PGOOD signal.

SYSRESET

The SYSRESET signal changes from LOW to HIGH (HCT logic level) at least 200 ms (T1) after the 5.2-V output voltage has reached 95% of its nominal value on switching on.

The SYSRESET signal changes to LOW after the 5.2-V output voltage has dropped to 95% of its nominal value.



Timing of SYSRESET:

Line trigger

LINETRIG
Output with squarewave signal (HCT logic level) with current line frequency.

7.2 Measuring Instruments and Auxiliary Equipment

Item	Type of Instrument	Specifications	Appropriate R&S device	Order No.
1	Digital voltmeter	DC to 30 V, 0.2%	UDS5	349.1510.02
2	20A Shunt	max. 20 A	UDL4-Z2	346.8065.02
3	Adjustable load	0 to 20 A / 28 V / 100 W		
4	Storage oscilloscope	1 V/Div 100 ms/Div		
5	Adjustable voltage source	0 to 4 V DC	NGPS	192.0061.02

7.3 Troubleshooting

7.3.1 Testing the Interfaces

Connector

Interface power supply (cable/plug)	W20/X20	W21/X21	W23/X23
Interface FSE (Motherboard)	X17	X18	X58

☞ **The power supply only operates if the following conditions are fulfilled at the interfaces:**

Item	Interface	Value range	Meaning
1	AC supply input	90VAC to 264 VAC Power switch to "ON"	
2	X17.4	<0.5 V	Activation input: is connected to ground by setting the Standby/On switch on the front panel of the FSE to the On position
3	X17.5	<±0.5 V	Reference potential for ext. temperature sensor (connected to ground on the RF Converter)
4	X17.6	<3.48 V referred to X17.5	Temperature voltage (Connected to temperature sensor on the RF Converter). If a higher voltage is applied, connect X17.6 to X17.5 for checking
5	X18.5	Load >0.1 A	Minimum load at +15 V, ground X18.4
6	X58.1	Load >2 A	Minimum load at +5.2 V, ground X58.9
7	All output voltages	Load < lower limit Current limiting according to table 7.1.3_1	Load smaller than guaranteed lower limit of current limiting

As to item 5/6
Generally fulfilled (if an analog module and computer section are installed); otherwise solder load to motherboard.

As to item 7
It is possible that one or several voltages are overloaded due to a faulty module. In this case, the power supply switches off all outputs. To be able to check which voltage has failed, connect X17.12 to ground by inserting a jumper on X16.

The power supply is not switched off on overload if jumper X16 is inserted. The current defined by the current limiting continuously flows. This may cause big damage due to the high currents flowing on the respective module. Therfore, this operating status should only be set as long as necessary for the measurements.

Subsequently, the faulty module can be determined by pulling out modules.

7.3.2 Error Symptoms

Disturbance	Cause
All output voltages including 12-V standby are missing	Power fuses F1/F2 faulty. PFC or auxiliary converter in power supply faulty.
All output voltages missing, 12-V standby available.	Standby applied to High (X20.4) (→ Connection to switch on front panel) Temperature voltage X20.5-X20.6 >3.48 V (→RF Converter too hot or not plugged in, or temperature sensor faulty) Main converter of power supply faulty
Power supply switches off immediately after switching on.	Overvoltage protection responds. → Voltage is increased due to faulty regulator in the power supply or due to a faulty module in the FSE. (e.g. connection between +5.5 V and +15 V).
Power supply switches off all output voltages (except 12-V standby) after approx. 5 to 15 s.	One output voltage is missing, power supply switches off (see below).
After connecting X20.12 to ground (jumper on X16 on motherboard): One or several output voltages are missing.	Outputs overloaded (→ faulty module). Respective regulators in power supply faulty.
Instrument switches off after a few minutes	Power supply is not sufficiently ventilated (e.g. faulty fan or ventilation holes impeded) or instrument is not sufficiently ventilated (temperature voltage > 3.48 V)

7.4 Testing the Specifications

Disconnect power supply from the motherboard

Connect X20.4 to ground (X23.9)
Connect X20.5 to ground (X23.9)
Connect X20.6 to adjustable voltage source 0 to 4 V, ground to X20.5 (set to 0 V first)
Connect X20.12 to ground
Connect load 150 Ω / 1.5 W to X21.5 and X21.4
Connect load 2.7 Ω / 10 W to X23.1 and X23.9

- Load the outputs with adjustable load and check the individual output voltages according to table 7.1.3_1 using a voltmeter. The specified voltage must be applied until the lower limit of the current limiting is reached. In the case of overload, the current must not exceed the upper limit. Take into account the base load due to the resistors!
Particular features of curent limiting at 28 V and 5.2 V see below 7.1.3.
The power supply must not switch off even if an output is overloaded for a longer period of time.

- Leave X20.12 open:
If an output is overloaded, the power supply must switch off all outputs except 12-V standby after approx. 5 to 15 s.

- The fan voltage (X20.8 - X20.9) must correspond to the voltage between X20.5 and X20.6 according to the characteristic below 7.1.3. Use an adjustable voltage source for checking.
If 3.350 ±0.025 V are applied between X20.5 and X20.6, the power supply must switch off (except 12 V Standby).

- Leave activation input X20.4 open! Voltage is only applied to the 12-V standby output (X23.5).
Reconnect X20.4 to ground.

- Switch power switch off and on, check SYSRESET using storage oscilloscope (X20.1), timing see 7.1.3

- Check LINETRIG using oscilloscope (X20.3): line-synchronous TTL signal

- Check PGOOD (X20.2) : TTL Low level, LED in rear panel must be illuminated.

7.5 Final Testing

Power supply installed in properly functioning FSE

There must not be any jumper on X16 (motherboard)!

Standby/On switch to standby,
Power switch to On,
Standby LED must be illuminated.

Standby/On switch to On,
Standby LED is extinguished, On LED must be illuminated,
Supply Check LED in power supply (rear panel) must be illuminated,
both fans in the power supply must be running, both fans in the FSE must be running, but must not run up (fan voltage with cold instrument 8 ±0.5 V),
FSE must boot.
Switch trigger to LINE,
FSE must sweep (trigger LED flashes).

Switch power switch off and on again after a few seconds.
The previous status must be set again.

7.6 External Interfaces

Pin	Signal name	D	T	Value range	Function / Remark
X20.1	SYSRESET-N	A	D	HCT	Reset signal for connected hardware. The SYSRESET signal changes from LOW to HIGH at least 200ms after the 5.2-V output voltage has reached 95% of its nominal value when switching on. On switch-off, the SYSRESET signal changes to LOW after the 5.2-V output voltage has dropped to 95% of its nominal value.
X20.2	PGOOD-P	A	D	HCT	Status signal indicating that an output voltage has dropped. The PGOOD signal changes from High to Low when switching on after all output voltages have rached 90% of their nominal value. The PGOOD signal changes from Low to High as soon as an output voltage falls below 90% of its nominal value. The fan voltage is not monitored. An LED in the rear panel of the power supply is illuminated simultaneously with the Low status of the PGOOD signal.
X20.3	LINETRIG	A	D	HCT	TTL signal with line frequency.
X20.4	ON-N	E	D	HCT	Activation input: If the power supply is connected to the AC supply voltage, it can be activated by connecting the activation input ON to GNDD or GNDA. The power supply is also activated if ON is connected to GNDD or GNDA and the power supply is then connected to the AC supply voltage. For deactivation, it is sufficient to leave the ON line open. The output VS12-P (Standby voltage) is activated irrespective of the activation input, if the power supply is connected to the AC supply voltage. On deactivation, the monitoring signals show the same behaviour as in the case of a power failure.
X20.5	TEMPFEGND	E	A	<±0,2 V	Ground of temperature sensor (see X20.6)
X20.6	TEMPFE	E	A	typ. 1 mA +10 mV/K	Supply (typ. 1mA) of temperature sensor (e.g. LM335) outside the power supply. The voltage at the temperature sensor (TEMPFE referred to TEMPFEGND) must be +10mV/K depending on the absolute temperature. The voltage applied to TEMPFE is used to control the voltage for the fans as well as to switch off in the case of overtemperature.
X20.7/9	FANGND	A	A		Ground for fans
X20.8/ 10	FAN	A	A	+8 to +15 V <0.8 A	Supply voltage for fans Voltage depends on temperature voltage at TEMPFE: Up to a temperature of 30°C ↔ 3.03 V the fan voltage is 8 ±0.5 V. At a temperature of 51°C ↔ 3.24 V, the fan voltage is 12±1V. Between these temperatures, the fan voltage increases proportionally to the temperature. If 51°C are exceeded, the voltage rises further up to max. 15 V.
X20.11	vacant				

Pin	Signal name	D	T	Value range	Function / Remark
X20.12	AUTOPS	E	D	HCT	Inhibition of automatic shutdown in the case of error (for service) If this control line is connected to GNDD or GNDA, there is no switch-off of all output voltages in the case of a) overtemperature at temperature sensor (voltage at TEMPFE >3.53 V) b) overload, short circuit or failure of an output voltage for more than 5 seconds.
X20.13-16	vacant				

Pin	Signal name	D	T	Value range	Function / Remark
X21.1-2	VA5-P	A	V	+5.5 ±0.05 V <2.7 A	Output voltage analog +5.5 V
X21.3-4	GNDA				Analog ground
X21.5-6	VA15-P	A	V	+15 ±0.1 V <6.7A	Output voltage analog +15 V
X21.7	GNDA				Analog ground
X21.8	VA15-N	A	V	-15 ±0.1 V <2.2 A	Output voltage analog -15 V
X21.9	GNDA				Analog ground
X21.10	VA28-P	A	V	+28 ±1 V <0.35 A	Output voltage analog +28 V

Pin	Signal name	R	A	Value range	Function / Remark
X23.1-3	VD5-P	A	V	+5.2±0.05 V <17A	Output voltage digital +5.2 V
X23.4	GNDD				Digital ground
X23.5	VS12-P	A	V	+12 ±0.3 V <0.25 A	Output voltage Standby +12 V This voltage is available as soon as the power supply is connected to the AC supply voltage irrespective of the activation input.
X23.6	VD12-P	A	V	+12 ±0.3 V <3.4 A	Output voltage digital +12 V
X23.7-9	GNDD				Digital ground

Pin	Signal name	R	A	Value range	Function / Remark
Power input	LINE	E	V	90 to 132 VAC <5 A 47 to 440 Hz 180 to 264 VAC <2.5A 47 to 66 Hz	Autoranging Power factor correction according to IEC555-2 / VDE 0838-2 Fuses 2x IEC127 T6,3H

Entry in column D (Direction): *A = Output, E = Input, B = Bidirectional*
Entry in column T (Type) : *A = Analog, D = Digital, V = Supply*

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SERVICE DOCUMENTS
GRAPHICS

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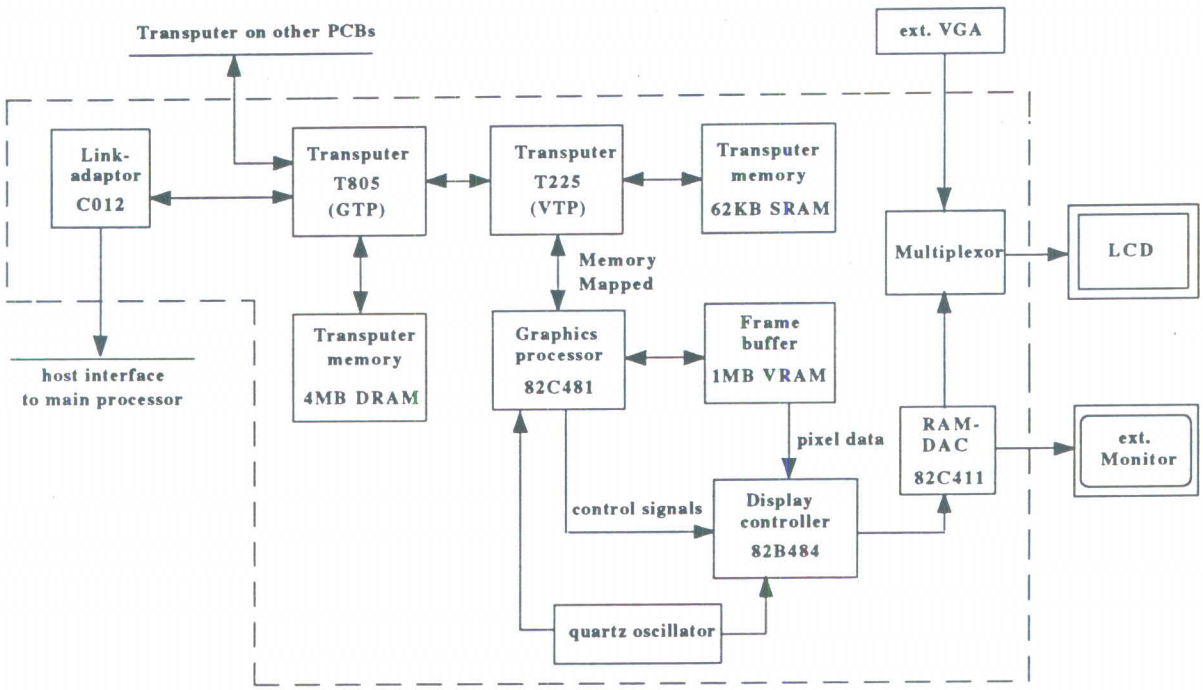
7 Testing the Module

7.1 Function Description

7.1.1 Block Diagram



7.1.2 Function inside the Instrument

The GRAPHICS module serves two purposes:

1. Generation of a fast graphical output for the measuring instrument and control of the internal LCD and of an external monitor. This function is implemented by a graphical subsystem consisting mainly of a 8514/A-compatible graphics processor and a special RAMDAC. Control of the internal LCD also includes the switchover between instrument and VGA display with the option FSE-B15 installed.
2. Interface inside the transputer network between main processor, the transputers on the other modules and the graphical subsystem. For this purpose, the module accommodates a PC link interface, two transputers and two slots for transputer modules (TRAMs).

7.2 Measuring Instruments and Auxiliary Equipment

Item	Type of instrument	Specifications	Appropriate R&S device	Order no.	Use
1	Digital voltmeter	0 to 20 V =	UDL35	1037.1807.02	- Testing the display supply voltage, - Level control
2	Oscilloscope	Limit frequency > = 60 MHz			Testing the control signals for display and monitor
3	VGA card	Separate output for LCD	from service kit		User interface of the test routine GR_CHECK.EXE
4	Test routine GR_CHECK.EXE				- Checks transputer network and graphics card, - Generates test patterns to determine the faulty module

7.3 Troubleshooting

A few seconds after switching on the isntrument, the internal display must show an initial picture with the message 'Rohde & Schwarz, Analyzer BIOS, Booting' and a rotating stroke. If this is not the case, the following tests can be carried out first

1. Does the display remain completely dark? (→ 7.3.2.1)
2. Doesn't the external montor show a picture either? (→ 7.3.2.2)
3. Does only the display show no picture or is the picture disturbed? (→ 7.3.2.3)
4. Does only the VGA screen appear on the display if the option FSE-B15 (controller function) is built-in ? (→ 7.3.2.4)

If the initial picture appears correctly, the rotating stroke should remain in any position for a short time and, again some time later, the previous text should be replaced by the message 'Transputer download successful'. If only the initial picture is to be seen even after a longer period of time has elapsed, the troubleshooting procedure is to be continued as described below 7.3.1.
If no fault has occurred so far, further messages of the type 'XXX download sucessful' or 'XXX download failed' must appear. If one of these messages is missing or 'failed' is displayed, this is probably due to a fault during initialization of the instrument hardware. In cases of doubt, it is recommended to proceed as described below 7.3.1.

If the instrument works properly until the screen is displayed (grid, softkeys etc.) and an error occurs subsequently, two cases are of interest in conjunction with the GRAPHICS module:

1. The display shows a fault in particular areas or with particular colours (→ 7.3.2.3).
2. The display is correct, however the external monitor shows a faulty picture or none at all (→7.3.3).

Other hardware errors of the GRAPHICS module should already become obvious during booting and are to be investigated as described above. In the case of doubt, the test routine GR_CHECK.EXE (→ 7.4.1) can always be used.

7.3.1 Transputer Software is not loaded

If problems occur when loading the transputer software, this may be due to different causes:

1. The main processor does not boot correctly or an error already occurs when loading the RMX software. (see section Main Processor)
   Symptoms:
   Even with the controller option FSE-B15 installed, it is not possible to boot from the floppy disk.
   Even after a longer waiting period, the instrument does not show any activity except for the rotating stroke of the initial picture.
2. There is a hardware error on the GRAPHICS module.
   Symptom: A white display appears instead of the initial picture.
3. One of the transputers or their series-connected hardware on the modules FRAC-SYN or Detector are faulty.
   Symptom: The initial picture appears correctly, however the message 'Transputer download successful' or one of the subsequent messages is missing.

Cases 2. and 3. can be investigated in greater detail using the test routine GR_CHECK.EXE (→ 7.4.1).

7.3.2 Problems with the LCD

7.3.2.1 Display remains dark

If the display remains dark after switching on, check whether the backlighting has been activated. This is the case if a narrow light stripe is visible at the upper or lower edge of the display. The best way to see whether the backlighting is switched on is to look at the rear of the display when the instrument is open. Possible causes of errors in the backlighting control can be obtained from the section Front Panel.

7.3.2.2 No Picture on Display and External Monitor

If neither the display nor the external monitor show a picture after switching on, the troubleshooting procedure should be continued using the test routine GR_CHECK.EXE (→ 7.4.1).
If, however, the initial picture disappears during booting and no picture is then shown neither on the display nor on the external monitor, this may be due to a hardware error or a faulty colour setting. This may happen e.g. if all display objects (grid, texts, marker, traces etc.) have been set to the colour of the background.

7.3.2.3 Display shows faulty picture or none at all

If there is only a white or disturbed picture on the display, although the external monitor shows a correct picture, the fault probably lies in the display control.
In this case, the connection cable from the display to the analog motherboard should be checked first. If this is okay, check the signals at the display connector on the analog motherboard or at multipoint connector X311 on the digital motherboard (→ 7.5). A voltmeter and an oscilloscope are required for this purpose. Besides, the test routine GR_CHECK.EXE (→ 7.4.1) should be started.
The signals HSync, VSync, Enable, Clock and the supply voltage should be checked first.
If none of these signals is correct, the signals DisplayOn and 8514ON should be checked next. Both are TTL signals coming from the digital motherboard. They are to be found at the following connector pins:

DisplayON: X311.A3
8514ON: X311.C3

The following combinations are obtained taking into account jumper X1 on the GRAPHICS module:

X1	DisplayON	8514ON	Display
	L	x	off
1-2	H	L	VGA
1-2	H	H	Instrument screen
2-3	H	L	off
2-3	H	H	Instrument screen

If these signals do not comply with the specifications, continue the troubleshooting procedure on the digital motherboard (see appropriate section), otherwise the GRAPHICS module is faulty.
If no faulty signal has been found so far, a test pattern should be used for further troubleshooting. The vertical striated pattern generated by the program GR_CHECK.EXE (→ 7.4.1) is especially suitable for this purpose. Each display line consists of 2 alternating white and black pixels. Thus a squarewave signal with a frequency of 6.29 MHz must be applied at the connector pins of the signals Red, Green und Blue Bit 0 to 2 (→ 7.5).

If these signals are also correct, the display must be assumed to be faulty, otherwise the fault is to be looked for on the GRAPHICS module.

7.3.2.4 Display only shows VGA Screen

If, with the controller option FSE-B15 installed, only the VGA screen is displayed on the internal display after switching on, a distinction is to be made between two cases:

1. A connected external monitor remains dark or shows a faulty picture, then proceed as described under 7.3.2.2.
2. The external monitor first shows the initial pattern and then the instrument screen. As a result, a fault in the display switchover is involved.

In the second case, the signals DisplayON and 8514ON (→ 7.3.2.3) should be checked.
If both signals are applied correctly, a hardware error on the GRAPHICS module is to be assumed.
If the signals do not comply with the specifications, continue the troubleshooting procedure on the digitial motherboard (see appropriate section).

7.3.2.5 Display never shows VGA Screen

If, with the controller option FSE-B15 installed, no VGA screen is shown on the display (in spite of switchover according to operating manual), the signals DisplayON and 8514ON (→ 7.3.2.3) should be checked. Besides, make sure that jumper X1 on the GRAPHICS module is at position 1-2.
Further error causes are to be found in the section VGA Option.

7.3.3 Problems with the External Monitor

An external monitor can be connected to each instrument and must always show the instrument screen (irrespective of the display mode). The signals for the monitor are generated on the GRAPHICS module and applied to the rear panel via the digital motherboard.
If there are problems with the external monitor, the connections listed below should be checked using an ohmmeter. If they are okay, the fault lies on the GRAPHICS module.

Signal:	HSync	Vsync	Red	Green	Blue	Ground
Rear panel ext. monitor	Pin 13	Pin 14	Pin 1	Pin 2	Pin 3	Pin 6, 7, 8, 10
GRAPHICS: X311	A15	C15	A16	B16	C16	A17, B17, C17

7.4 Testing the Specifications

7.4.1 Using the Test Routine GR_CHECK.EXE

The routine GR_CHECK.EXE is part of the service kit, supporting the troubleshooting procedure on the GRAPHICS module and the front panel.
The test routine assumes that a VGA card is installed in the instrument. This is the case for all instruments with the computer option FSE-B15 installed. In the case of instruments without this option, the VGA card from the service kit must be installed. An external monitor must be connected to the VGA card so that the program messages can be seen.
It is recommended to start the program from the DOS boot disk.
The individual functions of the test program will be explained in the following sections.

7.4.1.1 Testing the Transputer Network

Immediately after starting the program GR_CHECK.EXE the transputer network is automatically checked. Messages are displayed in the following format:

Test Transputer XXX ... pass or
Test Transputer XXX ... fail

The transputers are located on different modules:

Transputer:	GTP	FTP	PTP	VTP
Module	GRAPHICS	FRAC-SYN	Detector	GRAPHICS

The GTP is the central transputer, i.e. if the message 'fail' already apppears when it is tested, the other transputers cannot be correctly tested either. Testing of the graphics hardware can only be started if testing of the GTP and the VTP is positive. If the FTP or the PTP does not work properly, the troubleshooting procedure must be continued on the respective modules.

7.4.1.2 Testing the Graphics Hardware

After termination of the transputer test, the graphics hardware is initialized and tested by reading back the hardware registers, the following message being displayed on the VGA monitor:

Test GRAPHICS Hardware ... pass or
Test GRAPHICS Hardware ... fail

This message should simultaneously be visible on the display.
For this purpose, the test routine applies the signals 8514ON and DisplayON (→ 7.3.2.3) to High and additionally sets the backlighting to maximum brightness.

7.4.1.3 Test Patterns for Checking Display and External Monitor

After testing the graphics hardware, the VGA monitor displays a menu that allows to select various test patterns. These permit to make a distinction between a fault in the GRAPHICS module or in the display.
All test patterns are simultaneously shown on the display and on the external monitor.
The signals described in the following table are generated by the GRAPHICS module. If they are not correct, the fault lies in this module. If the test pattern is only displayed with faulty or not at all, although the signals are okay, the display is assumed to be faulty.

Test pattern	Analyses
Vertical striated pattern	The signals Red, Green, Blue Bit 0 to 2 (→ 7.5) can be checked. A squarewave signal with a frequency of 6.29 MHz must be applied there while the Enable signal is applied to high.
Black screen	The signals Red, Green, Blue Bit 0 to 2 (→ 7.5) must always be applied to low (Monochrome display: High). The display can be checked for faulty pixels.
White screen	The signals Red, Green, Blue bit 0 to 2 (→ 7.5) must be applied to high (Monochrome display: Low) as long as the enable signal is set to high. The display can be checked for faulty pixels.

7.4.2 Replacing the GRAPHICS Module

When replacing the module, note the correct position of jumper X11:

X11:	1-2	2-3
Type of display:	Monochrome	Color

7.5 External Interfaces

Type of display	Plug	Pin	Signal	Specification
Color display	X11 X311	2, 6, 10, 14, 16, 19 A23, B23, C23, A32, B32, C32	Ground	
	X11 X311	18, 22 A1	Vcc	+5 V ±5%
	X11 X311	15 A31	HSync	a 3.8-µs long TTL low pulse every 31.7 µs
	X11 X311	17 B31	VSync	a 64-µs long TTL low pulse every 16.7 ms
	X11 X311	21 C31	Enable	a 25.4-µs long TTL high pulse every 31.7 µs
	X11 X311	1 A24	Clock	25.175-MHz TTL squarewave signal with duty cycle 1:1
	X11 X311	3, 4, 5 A25, B25, C25	Red bit 0 to 2	TTL level
	X11 X311	7, 8, 9 A27, B27, C27	Green bit 0 to 2	TTL level
	X11 X311	11, 12, 13 A29, B29, C29	Blue bit 0 to 2	TTL level
Monochrome display	X12 X311	1, 5, 6, 8, 13, 16 A23, B23, C23, A32, B32, C32	Ground	
	X12 X311	3, 4 A1	Vcc	+5 V ±5%
	X12 X311	9 A31	HSync	a short TTL high pulse every 31.7 µs
	X12 X311	10 B31	VSync	a 31.7-µs long TTL high pulse every 16.7 ms
	X12 X311	2 C31	Enable	a 25.4-µs long TTL high pulse every 31.7 µs
	X12 X311	7 A24	Clock	12.88-MHz TTL squarewave signal with duty cycle 1:1
	X12 X311	14, 15, 17 A25, B25, C25	Red bit 0 to2	TTL level
	X12 X311	18, 11, 12 A27, B27, C27	Green bit 0 to 2	TTL level

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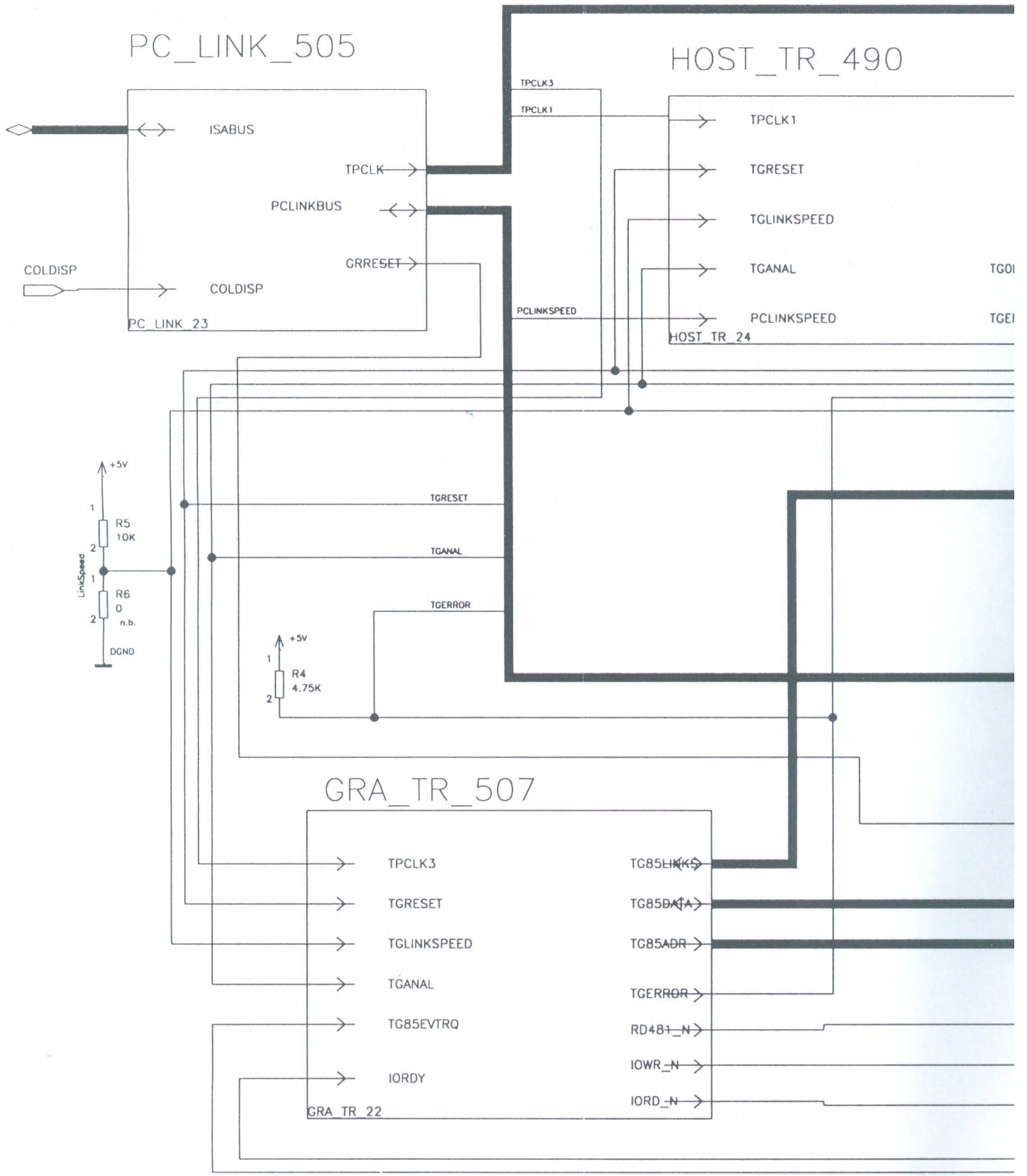
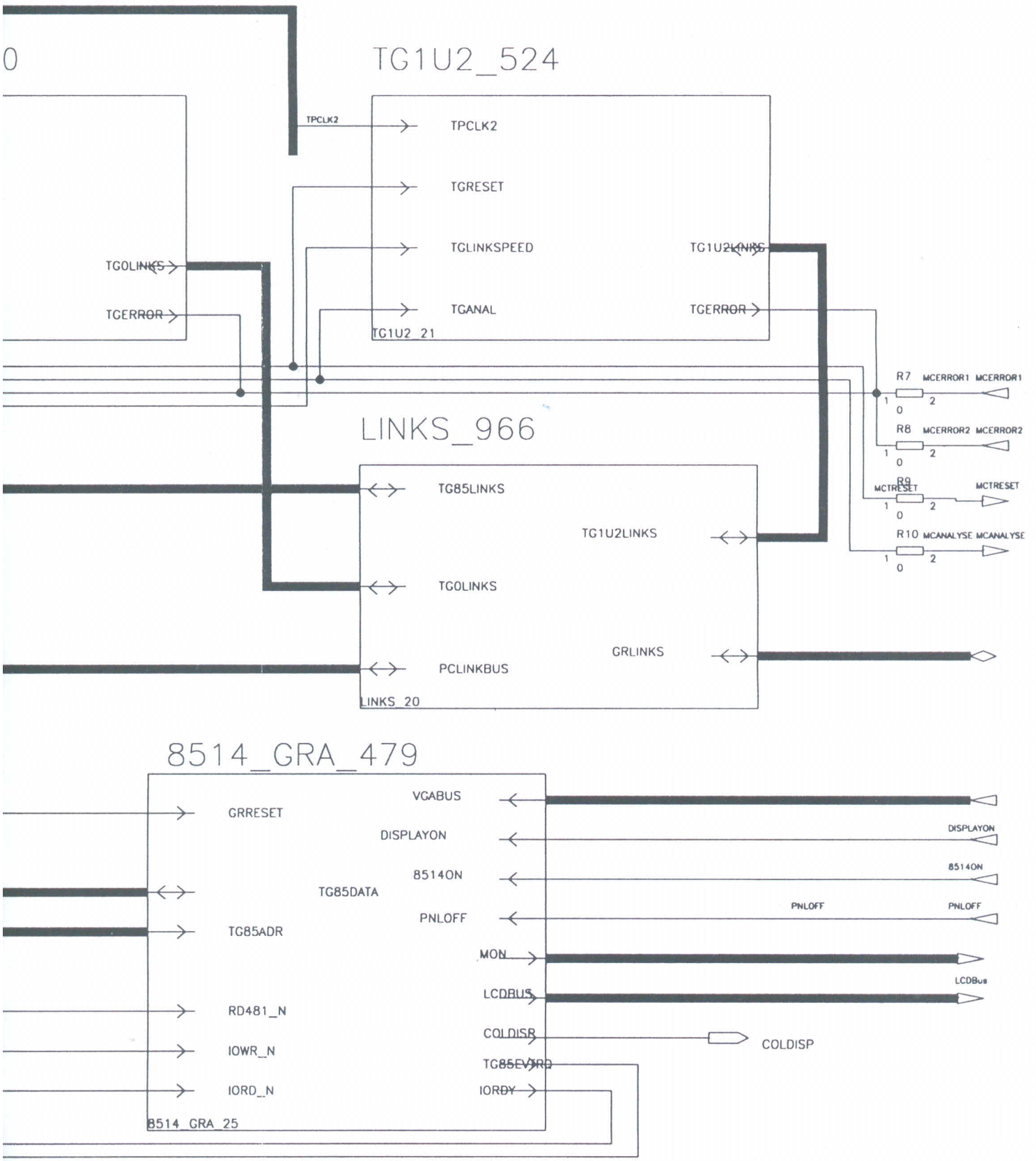
Stromläufe
Bestückungspläne
Circuit diagrams
Components plans
Schémas de circuit
Plans des composants

(R 29500 Bl 4)
095.1000 Bl. 4



ACHTUNG: EGB !
ELEKTROSTATISCH GEFAEHRDETE BAUELEMENTE ERFORDERN EINE BESONDERE HANDHABUNG.
ATTENTION ESD !
ELECTROSTATIC SENSITIVE DEVICES REQUIRE A SPECIAL HANDLING



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VGA

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7 Testing the Module

7.1 Function Description

The VGA module is part of the computer option FSE-B15. In addition to an external monitor, it can also control the internal LCD. It is inserted into one of the ISA-bus slots and additionally connected via a 50-pin flat cable to the digital motherboard. The signals are taken via this cable to the GRAPHICS module first for display control. The GRAPHICS module either displays the screen of the measuring instrument or the picture of the VGA card on the display.
The output of the VGA card for connection of the external monitor is applied via a special adapter cable to the rear panel of the instrument.

7.2 Troubleshooting

A built-in VGA card should already display a picture on a connected monitor during booting of the main processor. If this is not the case, the adapter cable to the rear panel of the instrument should be checked first. If no further error occurs during booting (→ section about main processor) and if no picture is displayed on the VGA monitor althought the adapter cable functions properly, the VGA card is probably faulty.
If a picture appears on the connected monitor, it should be possible to switch the display to the VGA picture if the computer option FSE-B15 is properly installed. Two errors may occur in this case:

1. The switchover does not affect the display:

   The fault probably lies in the switching logic (→ section about GRAPHICS module).

2. After switching over, a different but faulty picture can be seen on the display:

   The fault probably lies in the VGA card or in the 50-pin flat cable between VGA card and digital motherboard.